

Power Amplifiers, Trends and Design Challenges for the Upcoming Future

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Abstract—In this report, the main results of the research activities carried out within the 2025 MTT-S Graduate Fellowship Program, on the topic “Power amplifiers, trends and design challenges for the upcoming future”, are presented. Doherty power amplifier prototypes for different applications, implemented using various technologies, have been successfully demonstrated over operating frequencies ranging from sub-6 GHz up to the Ka-band.

Index Terms—Doherty Power Amplifier, GaN technology, GaAs technology, WiFi 6, class F, Ka-band.

I. INTRODUCTION

Power amplifiers (PAs) are fundamental components in radio-frequency front-ends (RFFE) for wireless communications, critically influencing the performance of multiple-input multiple-output (MIMO) systems, base stations, satellite payloads, and user terminals. As the final stage in the transmitter chain, the PA must deliver high output power while directly affecting system reliability and energy consumption.

In recent years, wireless systems have faced rapidly increasing data traffic per device and a growing demand for ultra-reliable, low-latency communications (URLLC) with very high transmission rates [1]. As a consequence, the next generation of wireless systems will require PAs to meet increasingly stringent design challenges.

The push towards higher operating frequencies and highly integrated architectures amplifies the impact of parasitic elements, limiting gain, bandwidth and efficiency. Furthermore, modern communication systems employ complex modulation schemes with very large Peak-to-Average-Power Ratios (PAPR), necessitating PAs capable of efficient operation under significant output power back-off. High linearity is equally crucial, as nonlinear distortions can severely degrade the reliability of communication. Although digital predistortion (DPD) techniques can compensate for certain nonlinear effects, they are costly and complex to implement, thus intrinsic linearity optimization remains essential.

The Doherty Power Amplifier (DPA), which exploits the load modulation technique, has already been proved to be one of the most promising PA architectures, as it provides a good compromise between design complexity and the efficiency-linearity trade-off when handling high-PAPR signals [2].

In this context, the research activity focused on several Doherty Power Amplifier design solutions aimed at meeting the requirements of modern wireless communication systems. The following sections briefly discuss the project outcomes, based on the realization of integrated DPA prototypes designed for various scenarios and different technologies.

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II. PROJECT OUTCOMES

A. DPA for WiFi 6 communication systems

WiFi 6 standard (802.11ax) was introduced to increase bandwidth and incorporate advanced technologies (MU-MIMO, OFDMA, 1024-QAM) to improve communication speeds while efficiently managing multiple users [3]. In this context, where an extremely low level of EVM is required in operating conditions, the effectiveness of the DPA architecture is evaluated in combination with high-linear HBT GaAs technology. An integrated three-stage DPA prototype was realized covering the 5-6 GHz frequency band, which microscope photograph is shown in Fig.1. Transistors were grouped in power cells to realize the final stage of the Carrier and Peaking branch. The DPA combiner is carefully implemented to address the low optimum impedance values required in the final stages. Two cascaded drivers were adopted to maximize the gain and enable operation at low EVM levels. Also, bias points of driver devices were optimized to achieve a flat AMAM behavior.

The fabricated MMIC provides an output power of 32 dBm along with 22.5 dB of gain across the 5-6.2 GHz frequency range, reaching a peak PAE of 44 %. Linearity tests using a 20 MHz MCS11 signal indicated a maximum EVM of -24 dB at an output power of 22 dBm, with PAE approaching 11 % at 5.6 GHz [4].

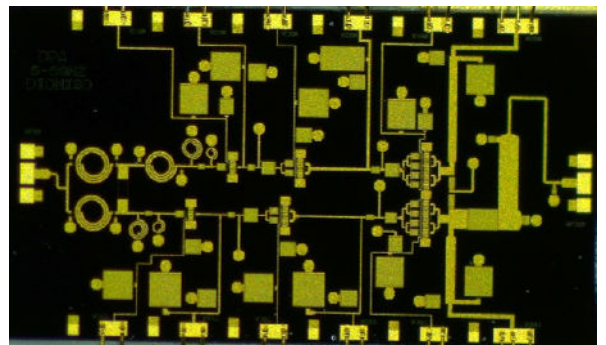


Fig. 1. Picture of the MMIC DPA for WiFi 6 applications in HBT GaAs technology (size: 4.5 mm x 2.5 mm).

B. X-band Harmonic tuned DPA

Advanced harmonic manipulation strategies were also explored as a means to enhance the performance of the DPA architecture. In [5], a class F design strategy was adopted for both Carrier and Peaking branches. Typically, due to class C bias condition, it is not possible to enable class F proper operation in the Peaking amplifier, as the third

harmonic generated at its output shows a not-favorable phase relation with the fundamental component. In this work, the nonlinearities generated by a driver stage are exploited to inject a third-harmonic component at the input of the Peaking, and to change the phase relation of the third harmonic generated at the output. The theoretical formulation was presented together with its experimental validation at both device and DPA level. The fabricated prototype in 120 nm GaN technology is shown in Fig.2.

The experimental results demonstrated the potential of the proposed approach, achieving a peak output power of 36 dBm, 40% efficiency at 10 GHz, with an extremely flat gain behavior. With an LTE modulation scheme, an ACPR of -30 dBc was obtained with an average output power of around 32 dBm and efficiency higher than 32%, highlighting the intrinsic linearity of the adopted strategy.

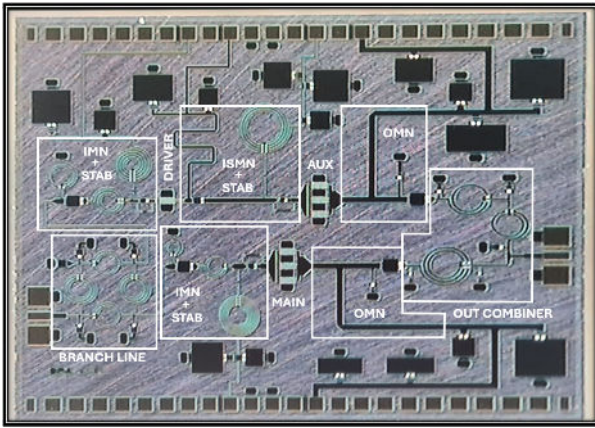


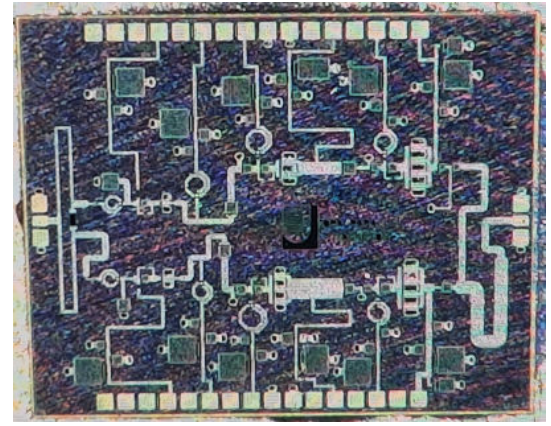
Fig. 2. Photograph of the MMIC GaN DPA prototype in full class F working condition (size: 3.65 mm x 3 mm).

C. Three-stage Ka-band DPA

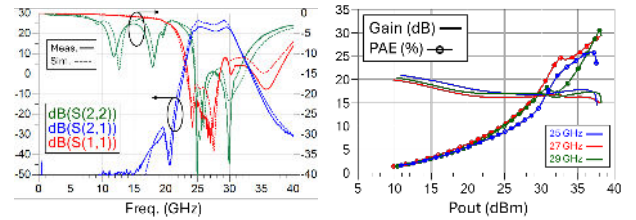
The Ka-band is of particular interest for 5G NR FR2 millimeter-wave communications and is widely considered a potential spectrum for beyond-5G and future 6G systems, thanks to the large available bandwidth enabling multi-gigabit data rates. Evaluating DPA performance in this band is critical due to the necessity of enhancing efficiency in the presence of highly modulated waveforms, but with parasitic effects becoming dominant at millimeter-wave frequencies. Within this scenario, a DPA working in Ka-band was designed and manufactured in 120 nm GaN technology. The DPA, shown in Fig.3a, is composed of a three stage architecture, with the output matching networks of the Carrier and Peaking devices that were carefully designed to compensate for the parasitic effects of the transistors. Measured scattering parameters demonstrate a small-signal gain higher than 20 dB from 24 to 30.5 GHz, with a fractional bandwidth of approximately 24% (Fig.3b). Large-signal performance indicate a PAE between 15% and 20% at 8 dB of output back-off, achieving a saturated output power of 38 dBm (Fig.3c).

III. IMPACT STATEMENT AND CAREER PLAN

I am honored to have been selected as a recipient of the 2025 IEEE MTT-S Graduate Fellowship, and I would like



(a)



(b)

(c)

Fig. 3. (a) Photograph of the MMIC GaN DPA operating in Ka-band (size: 3.5 mm x 2.8 mm), (b) small-signal performance and (c) large-signal performance.

to express my sincere gratitude for this opportunity. This award has represented for me not only a financial support that enabled me to participate more actively in international events, but also a strong encouragement that further strengthened my motivation to contribute to research and to the advancement of RFFE technologies for microwave electronics. Attending IMS 2025 in San Francisco also allowed me to feel part of the global community, broadened my perspective on current challenges and trends, and significantly enhanced my professional connections. As I enter the final year of my Ph.D., I am not yet certain whether I will pursue an academic career or enter industry, but I am committed to continuing work in this field and contributing to its advancement.

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