

Gain-Boosted N-Path Receiver with Embedded Passive Harmonic Suppression

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Abstract—Harmonic blockers pose a fundamental challenge in state-of-the-art widely tunable N-path filter-based receivers. This report presents a low-power solution that embeds passive harmonic rejection to knock out these blockers at the earliest opportunity in the front end. Fabricated in 22-nm FD-SOI technology, the prototype spans 0.25–3 GHz and achieves 29.5–32 dB gain with a 3.75–5.3 dB noise figure in a compact 0.048 mm² footprint while consuming 0.89 mW static power and 1.53 mW/GHz dynamic clock power. With harmonic blocker 1-dB compression points of -3/-2 dBm, the design delivers over 3× greater harmonic blocker resilience than prior state-of-the-art. This work was presented at RFIC 2025 and subsequently extended in an invited paper in the IEEE Journal of Solid-State Circuits.

Index Terms—Low power, IoT, N-path, Blocker tolerant, Harmonic Blocker, Software-defined radio.

I. INTRODUCTION

The next wave of Internet of Things (IoT) deployment—encompassing medical wearables, factory sensors, and urban monitoring cameras—will rely on wide-area cellular connectivity [1]. Multi-band support within a single low-cost transceiver demands a frequency-programmable receiver, which precludes the fixed-band LC filters found in legacy IoT standards such as Bluetooth Low Energy (BLE) and ZigBee [2].

N-path filters, composed solely of switches and capacitors, are a natural solution for low-cost reconfigurable receivers. This filtering scheme is readily amenable to miniaturization by exploiting the Miller effect—an architecture widely known as the gain-boosted N-path receiver [3]. Although low-power receivers based on this approach have been reported, all remain vulnerable to harmonic blockers [3], [4]. As shown in Fig. 1(a), in a conventional gain-boosted N-path topology, local-oscillator (LO) harmonics picked up by the antenna are amplified and can saturate the gain-stage output. This issue stems from the comb-filter nature of the N-path filter employed in the feedback path.

The harmonic-rejection (HR) extension that we proposed in [5], [6] addresses this limitation by directly suppressing the *driving-point impedance* of a one-port N-path filter at the LO harmonics. Consequently, harmonic blockers no longer act as the Achilles’ heel of the N-path circuit; instead, they are attenuated in the same manner as other out-of-band interferers. In this project, we aim to apply this network in feedback.

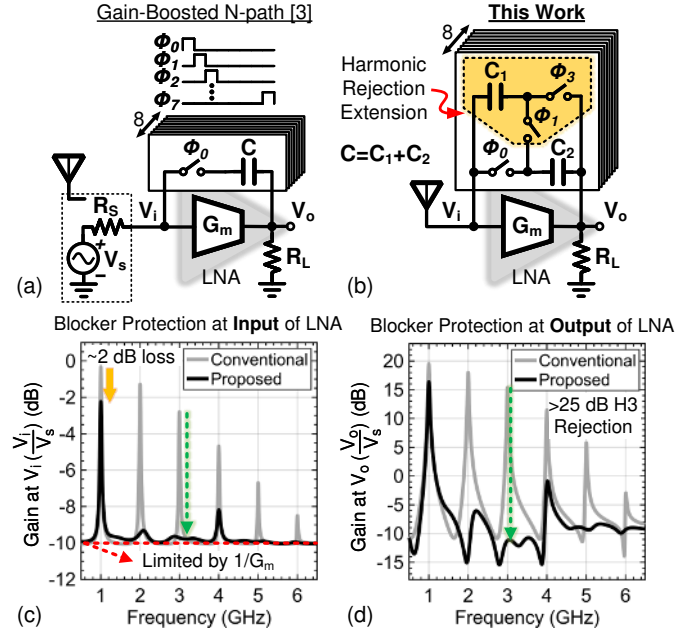


Fig. 1. (a) Conventional gain-boosted N-path architecture [3]. (b) Proposed harmonic-suppressing gain-boosted N-path RX. Simulated gain of the conventional and proposed designs at (c) the LNA input and (d) output for $G_m=40$ mS, $R_L=0.25$ k Ω , $C=2C_1=2C_2=1.5$ pF and $f_{LO}=1$ GHz.

Fig. 1(b) depicts the proposed harmonic-suppressing gain-boosted N-path receiver, which offers the following key advantages over [3]: incorporating the HR extension in the feedback path significantly enhances receiver linearity by protecting both the low-noise amplifier (LNA) (i) input and (ii) output from harmonic blockers (Fig. 1(c)–(d)), achieving a 3rd-harmonic blocker 1-dB compression point (B1dB) of -3 dBm under a 0.6 V supply. This work was first presented at RFIC 2025 [7] and subsequently extended in an invited paper in the IEEE Journal of Solid-State Circuits [8].

II. CIRCUIT IMPLEMENTATION AND PROJECT RESULTS

The proposed harmonic-suppressing gain-boosted N-path receiver, shown in Fig. 2, is implemented in a 22-nm FD-SOI technology. The receiver employs a resistive-feedback LNA followed by a harmonic-suppressing gain-boosted N-path network. A three-stage passive pipeline down-mixing is employed to extract the baseband signal while boosting the gain and HR passively. In conventional N-path layouts, the switches of each slice are placed adjacent to one another so that their source–drain connections remain local. However, because switches driven by the same clock phase are physically distributed across the layout, clock meshing is typically required to maintain phase uniformity. This meshing

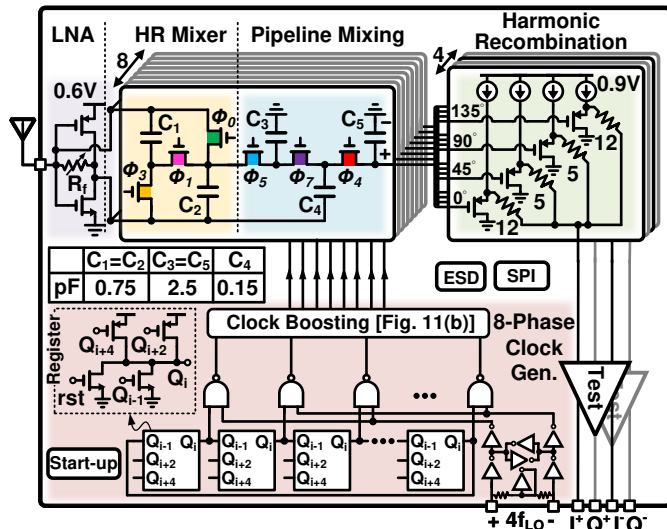


Fig. 2. Block diagram of the implemented harmonic-suppressing gain-boosted N-path RX with clock bootstrapping.

substantially increases the capacitive load on the boosted clock network, raising its power consumption. For instance, a parasitic wiring capacitance of 50 fF at each of the eight paths, driven with a boosted supply of 1.1 V, results in approximately 485 $\mu\text{W}/\text{GHz}$ of additional power dissipation (given by $NCV_{DD}^2 f$). Here, an alternative floorplan is adopted in which all switches sharing the same clock phase are placed adjacent to one another. Each phase is then routed through a single dedicated rail without meshing, significantly reducing parasitic capacitance and clock power.

The prototype occupies an active area of 0.048 mm^2 , as shown in Fig. 3(a). The power consumption at 1 GHz LO is 2.42 mW and the breakdown is reported in Fig. 3(b). The prototype operates across a wide frequency range of 0.25–3 GHz while achieving 29.5–32 dB gain and a 3.75–5.3 dB noise figure. As shown in Fig. 4(a), the measured harmonic rejection ratios of 63 dB and 62 dB are achieved for the third and fifth harmonics, respectively. As shown in Fig. 4(b), the receiver maintains strong blocker resilience, with harmonic B1dB values of -3 dBm and -2 dBm for third- and fifth-harmonic blockers, respectively. Simulation shows that disabling the harmonic-reset switching in the feedback path—i.e., removing the ϕ_1 switch in Fig. 2 to decouple bottom-plate and top-plate mixing in the HR mixer while leaving the rest of the circuit unchanged—reduces the H3 B1dB by 15 dB. Relative to the state-of-the-art widely tunable low-power receiver in [9], this work demonstrates over $3\times$ higher resilience to third-harmonic blockers.

III. FELLOWSHIP IMPACT AND CAREER PLAN

Receiving the MTT-S Graduate Fellowship has been a tremendous honor and has further strengthened my interest in developing blocker tolerant front-ends for future wireless communication systems. The opportunity to attend IMS 2025 exposed me to cutting-edge research in microwave and RF integrated circuits and allowed me to engage with researchers

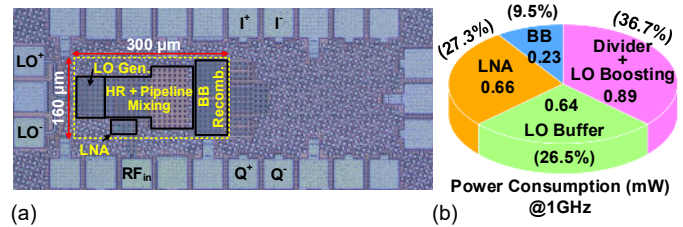


Fig. 3. (a) Die micrograph. (b) Power consumption breakdown at 1 GHz.

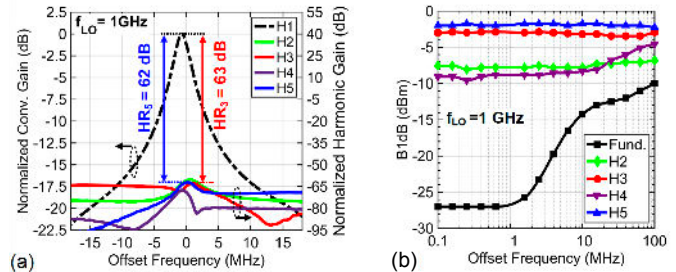


Fig. 4. (a) Measured normalized harmonic transfer functions at $f_{LO}=1$ GHz. (b) Measured B1dB and harmonic B1dB versus offset frequency at $f_{LO}=1$ GHz.

and industry professionals from across the field. Looking ahead, I plan to pursue a career in industry, translating circuit-level innovations into products that directly impact everyday life. I also look forward to remaining actively engaged with the MTT-S community through peer review, and mentoring future researchers in RF integrated circuit design.

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