

Broadband GaAs HBT Doherty Power Amplifier Using Lumped Compensation Network and Input Phase Correction for 5G Applications

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Abstract—This report presents the research outcomes supported by the 2024 IEEE MTT-S Graduate Fellowship Program, focusing on a broadband Gallium Arsenide (GaAs) heterojunction bipolar transistor (HBT) Doherty power amplifier (DPA) that employs a lumped compensation network (LCN) and input phase correction technique for 5G applications. A LCN is utilized with an integrated impedance inverter to enhance output power back-off (OBO) efficiency across a wide frequency range. To mitigate the overdrive issue caused by the LCN under saturation, and an on-chip coupler-based input phase correction network is introduced. The DPA is implemented using a $2\mu\text{m}$ GaAs HBT process and achieves broadband operation over 3.1–4.3 GHz, covering the 5G n77 and n78 bands. Measurement results demonstrate a saturated output power of 32.73–33.77 dBm with a saturated power-added efficiency (PAE) of 39.54%–46.51%. At 6 dB OBO, the DPA maintains a PAE of 30.84%–34.95%. When tested with a 100 MHz bandwidth 64-QAM signal with 5.6 dB PAPR, the DPA achieves an average PAE of up to 34.3% and an adjacent channel power ratio (ACPR) better than -45.2 dBc after digital predistortion (DPD).

Index Terms—5G, broadband, Doherty power amplifier (DPA), gallium arsenide (GaAs), heterojunction bipolar transistor (HBT), lumped compensation network (LCN), monolithic microwave integrated circuit (MMIC), phase correction.

I. INTRODUCTION

THE rapid development of wireless communications imposes stringent requirements on power amplifiers (PAs), which need high efficiency, wide bandwidth and good linearity for high-speed data transmission. As a promising candidate, the Doherty power amplifier (DPA) features high back-off efficiency, simple structure and high reliability, and has been widely applied in 5G systems. For 5G terminals and micro base stations, broadband, high-performance and low-cost hybrid integrated PAs based on Gallium Arsenide (GaAs) are highly demanded. Although existing GaAs DPAs have achieved favorable efficiency and bandwidth [1]–[6], the trade-off between bandwidth and efficiency still requires further research.

Targeting the bandwidth and efficiency demands of 5G NR, this paper proposes a novel broadband GaAs HBT DPA adopting a lumped compensation network (LCN) and input phase correction. The two-element LCN optimizes wideband load modulation to improve broadband performance. Meanwhile, an on-chip coupler-based phase correction network is designed to suppress the transistor overdrive caused by impedance variation at the combining node after deploying the LCN.

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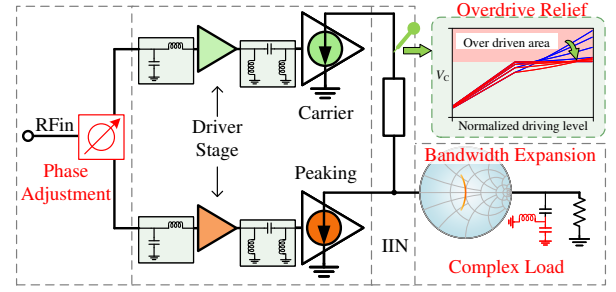


Fig. 1. Block diagram of the proposed DPA.

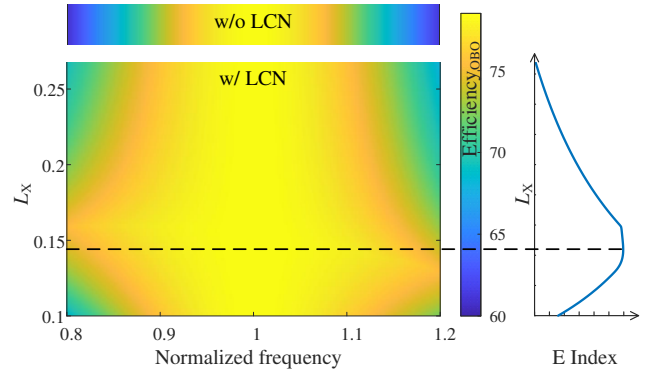


Fig. 2. OBO bandwidth performance of the proposed DPA before and after adding LCN.

II. PROJECT OUTCOME

The proposed DPA architecture is shown in Fig. 1. Similar to the traditional DPA structure, the carrier PA and the peaking PA are connected by an impedance inverting network (IIN). At the combining point, the post-matching network (PMN) is responsible for matching the load to $R_{\text{opt}}/2$ (in the case of a symmetric DPA). Additionally, a LCN composed of l_c parallel LC grounding network is also connected to the combining point through a DC-blocking capacitor to provide a frequency-dependent complex impedance. Fig. 2 illustrates the OBO bandwidth performance of the DPA before and after adding the LCN. Within the normalized frequency range of 0.8–1.2, after adding the LCN, the theoretical OBO efficiency of the DPA improves from 61.1%–78.5% to 73.8%–78.5%.

However, the LCN leads to transistor saturation overdrive, which degrades stability and narrows the saturation bandwidth of the DPA. This work suppresses the overdrive by tuning the

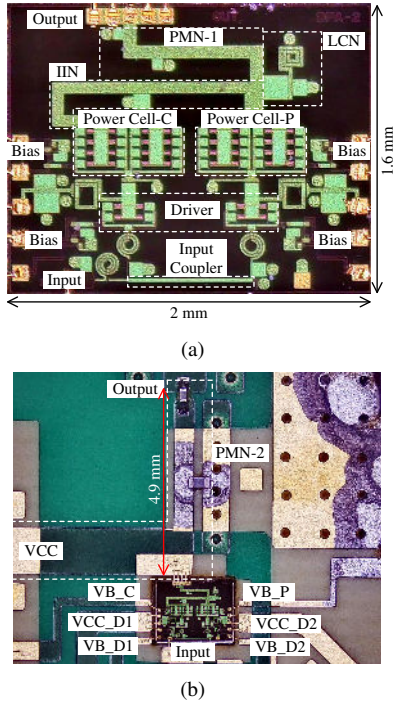


Fig. 3. Photograph of the implemented DPA. (a) GaAs MMIC. (b) Assembled evaluation board.

input phase difference between carrier and peaking PAs, while maintaining the wide OBO bandwidth from complex load impedance. This scheme barely affects the OBO performance. When the phase difference θ_p is set to -90° , the peaking PA works without overdrive across the normalized frequency of 0.8-1.2, with fundamental collector voltage amplitude of 1-1.04. Meanwhile, the carrier PA overdrive is greatly alleviated, whose voltage amplitude is 1-1.18 in the same band. This -90° phase shift can be simply realized by a coupler, avoiding dual-input structures.

For verification, a phase-corrected DPA with complex combining load is designed and simulated using WIN Semiconductor $2\ \mu\text{m}$ GaAs HBT process. The fabricated MMIC occupies $1.6 \times 2\ \text{mm}^2$, as shown in Fig. 3 and Fig. 3(a). The chip is mounted on a Rogers RO4350B substrate (20 mil thick) with a cavity layout and silver epoxy for better heat dissipation, as depicted in Fig. 3(b). Both continuous wave (CW) and wideband modulated signals are adopted for experimental measurement.

Fig. 4 presents both the measured power-added efficiency (PAE) and gain as functions of output power. The results demonstrate successful Doherty operation with 22.19 - 25.30 dB small signal gain across 3.1-4.3 GHz. The DPA delivers a saturated output power of 32.73-33.77 dBm with a PAE of 39.54%-46.51%. At 6 dB OBO, the PAE remains 30.84%-34.95%. These experimental results demonstrate that the proposed DPA achieves excellent overall performance in terms of gain, efficiency, and output power across a fractional bandwidth (FBW) exceeding 32%, fully covering the 5G n77 and n78 bands.

A 100 MHz bandwidth 64-QAM wideband signal with a PAPR of 5.6 dB is used as the excitation for testing the

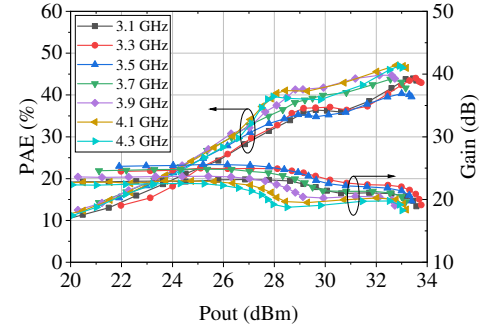


Fig. 4. Measured PAE and gains of the fabricated DPA versus output power at different frequencies.

fabricated DPA. The measured output spectra of the fabricated DPA at four frequencies: 3.15 GHz, 3.5 GHz, 3.9 GHz and 4.25 GHz, both with and without digital pre-distortion (DPD). The measured average output power ranges from 27 to 27.3 dBm, and the corresponding average PAE is between 30.8% and 34.3%. The adjacent channel power ratio (ACPR) before DPD is in the range of -25.9 to -31.3 dBc, and is significantly improved to between -45.2 and -48.8 dBc after applying DPD.

III. CAREER PLAN AND FELLOWSHIP IMPACT

I sincerely appreciate receiving the 2025 IEEE MTT-S Graduate Fellowship. With this support, I will continue my research on broadband high-efficiency PAs and MMIC design, publish quality papers and engage in academic exchanges. I aim to build a career as an RF/microwave engineer and researcher focusing on next-generation wireless communication technologies. This fellowship eases my financial pressure, strengthens my research confidence, and connects me to the global MTT-S community, greatly facilitating my long-term professional development.

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