A New CSWPL Behavioral Model for Microwave GaN Transistors Including DC Bias Voltages

Xiaoqiang Tang, and Jialin Cai, *Senior Member, IEEE*

***Abstract*—In this work, a novel frequency domain behavioral modeling approach for gallium-nitride (GaN) devices is presented. The proposed technique is based on using the canonical section-wise piecewise linear (CSWPL) model framework to interpolate the dc input and output bias voltages by a two-dimensional polynomial function. The basic theory associated with the developed model is described in detail and experimentally verified. The model is implemented in a commercial software and, then, validated through radio frequency (RF) tests with measured load-pull data from 6-W GaN devices. The achieved results demonstrate an excellent prediction capability, thereby proving the accuracy of the developed modeling methodology. Additionally, the proposed model is utilized for a broadband PA design for a further validation. The measurements carried out on the realized PA are compared with the simulations based on using the proposed model. The comparison is performed at four different bias conditions. The agreement between measurements and simulations confirms the extracted model's validity.**

***Index Terms*—CSWPL model, dc bias voltages, frequency-domain behavior, gallium nitride (GaN), power amplifier.**

I. Introduction

Radio frequency (RF) power amplifiers (PAs) play a key role in modern wireless communication systems [1]. During the past few decades, a series of high-efficiency PA architectures have been proposed [1]. In order to facilitate high-fidelity simulations of PA circuits for real-world performance, highly accurate transistor models are becoming increasingly essential. Meanwhile, to satisfy the PA design requirements, the model is requested to capture device behavior under various variables, such as frequency, input power, load conditions and DC bias voltages.

In this work, a novel dc-bias included CSWPL model employing polynomial fitting technique is theoretically developed and experimentally validate. The model incorporates both gate and drain voltages into the CSWPL model formulation, enabling the model to predict transistor behavior across a wide range of bias voltage conditions and under different input power levels with a single set of parameters. The model validation is accomplished using measured data of a 6-W GaN HEMT device. In addition, to further verify the proposed modeling technique, a broadband PA is successfully designed using the extracted model.

X. Tang was with the Key Laboratory of RF Circuit and System, Ministry of Education, Hangzhou Dianzi University, 310018 Hangzhou, China and now he is working as a Ph.D. student at the University of Aveiro.

J. Cai are with the Key Laboratory of RF Circuit and System, Ministry of Education, Hangzhou Dianzi University, 310018 Hangzhou, China. (e-mail: caijialin@hdu.edu.cn).

II. The New CSWPL Model Including DC-Bias: Theoretical Analysis

The CSWPL behavioral model for power transistors was firstly proposed in [2], where the CSWPL function was applied to the standard Cardiff model with the aim of overcoming the amplitude dependence of the large incident wave of the model.

A novel feature of the present study consists of the inclusion of DC bias information, both gate and drain bias voltages, in the formulation of the CSWPL model. For a two-port DUT, a two-dimensional polynomial function can be used to separate the DC bias stimulus terms from the RF term according to a general theory of mixing RF and DC bias inputs [3].

By applying the two-dimensional polynomial function, the dc-bias included CSWPL model can be obtained as follows [4]:

$$B_{pm} = P_1^m \sum_{l=-Lk_{11}=1k_{21}=1}^{l=L} \sum_{}^{N} \sum_{}^{N} F_{pm,l,k_{11},k_{21}}(DC\,Bias) \prod_{j=11}^{21} \varnothing_{k_j,j}\left(|A_j|\right)\left(\frac{Q_1}{P_1}\right)^l$$
$$= P_1^m \sum_{l=-Lk_{11}=1k_{21}=1}^{l=L} \sum_{}^{N} \sum_{}^{N} \sum_{u=0}^{U_{max}} \sum_{v=u}^{V_{max}} C_{pm,l,k_{11},k_{21},u,(v-u)} V_{gs}{}^{u} V_{ds}{}^{v-u} \prod_{j=11}^{21} \varnothing_{k_j,j}\left(|A_j|\right)\left(\frac{Q_1}{P_1}\right)^l \tag{1a}$$

where

$$\begin{aligned} \varnothing_{1,j}\left(|A_j|\right) &= 1 \\ \varnothing_{2,j}\left(|A_j|\right) &= |A_j| \\ \varnothing_{3,j}\left(|A_j|\right) &= \left||A_j| - \beta_{j,1}\right| \\ &\vdots \\ \varnothing_{N,j}\left(|A_j|\right) &= \left||A_j| - \beta_{j,N-2}\right| \end{aligned} \tag{1b}$$

III. Model Validation

Model validation is performed through laboratory tests, which is described below. The DUT is a 6-W, 6 × 75 um GaN HEMT device with a 0.25-μm gate length: the used test bench is a Keysight PNA-X N5247A combined with a focus microwave load-pull system. The proposed model is implemented in Keysight's Advanced Design System (ADS) with a frequency-domain defined (FDD) device.

Table I illustrates the B_{21} prediction performance of a dc-bias included CSWPL model. It is evident that when $U_{\max}$ and $V_{\max}$ are equal to 2, there is an optimal balance between model complexity and performance. The model's relative error is less than 1%, and its accuracy does not improve with

increasing model complexity.

TABLE I
AVERAGE RELATIVE ERROR OF DC-BIAS INCLUDED CSWPL MODEL WITH DIFFERENT MODEL COMPLEXITIES

Maximum Order of the V_{gs} (U_{max})	Maximum Order of the V_{ds} (V_{max})	Total Number of Model Parameters	Average Relative Error (%)
1	1	240	1.80
1	2	400	1.41
1	3	560	1.12
2	2	480	0.90
2	3	720	1.31
3	3	800	1.28

IV. MODEL APPLIED FOR BROADBAND PA DESIGN

In this section, the proposed model is exploited for the design of a broadband PA.

During the model extraction, the values of V_{gs} are from -3 V to -2 V with a step of 0.5 V, the values of V_{ds} vary from 20 V to 30 V with a step of 5 V, and the specific input power ranges from 20 dBm to 30 dBm with a 2-dB step.

A matching network is formed using stepped impedance structures, while a stabilization network is added to the matching circuit. The photo of the PA realized on a Rogers 4350B substrate is given in Fig. 1. Fig. 2 reports the performance comparison between the simulated and measured results. Output power (P_{del}), gain, and power added efficiency (PAE) are plotted against the input power ranging from 20 dBm to 30 dBm for the designed PA at four different bias conditions. As shown in Fig. 2, there is a good agreement between the measured and simulated results for all the four bias points.

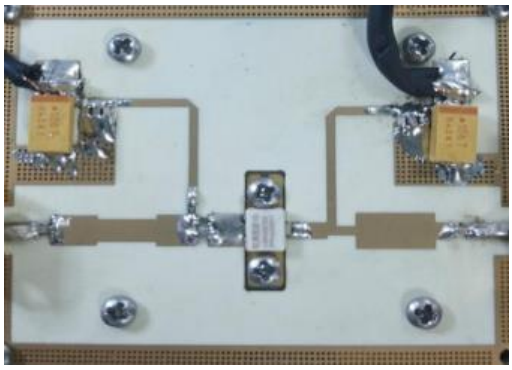

Fig. 1. Photo of the fabricated GaN-based PA.

V. CONCLUSION

A new bias included CSWPL model was developed and validated in this work. A two-dimensional polynomial function was used to interpolate the dc bias voltages into the standard CSWPL model. Comprehensive test examples of the model based on measured data were given, demonstrating an excellent prediction capability. The developed modeling methodology was further validated with its application to a broadband PA design. By comparing measured and simulated results, a good agreement was achieved, demonstrating that the proposed model can be successfully adopted for PA design.

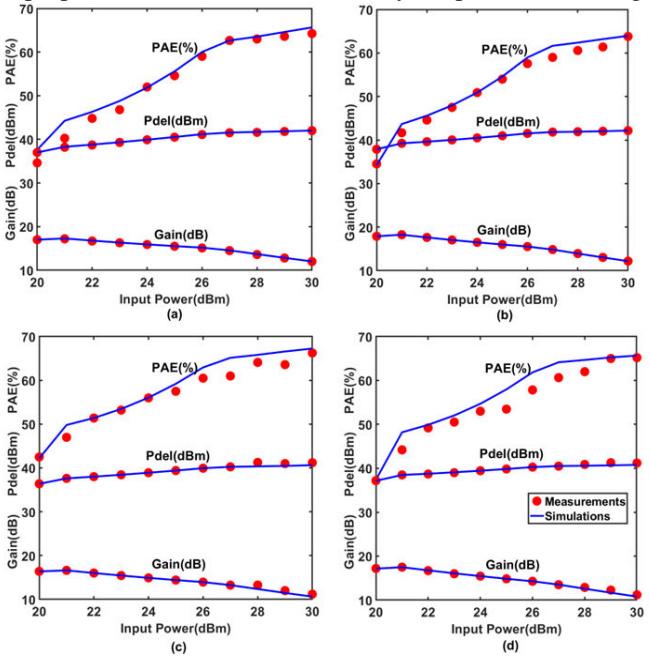

Fig. 2. Comparison of the measured (symbols) and simulated (solid lines) PAE, gain and P_{del} vs. input power for the fabricated broadband GaN-based PA under four different bias conditions: (a) V_{gs} =-2.7 V, V_{ds} =28 V, (b) V_{gs} =- 2.3 V, V_{ds} =28 V, (c) V_{gs} =-2.7 V, V_{ds} =23 V, and (d) V_{gs} =-2.3 V, V_{ds} =23 V.

VI. FUTURE PLAN AND IMPACT STATEMENT

After completing my Masters in Electrical Engineering, I have enrolled in the PhD program in Electrical Engineering at the University of Aveiro and I am excited to continue working in the field of device modeling under the guidance of Prof. J. C. Pedro. There is no doubt that the MTT-S Scholarship has had a significant impact on me, and the recognition from it has kept me fully interested in the field.

REFERENCES

[1] S. C. Cripps, *RF Power Amplifier for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech House, 2006.

[2] J. Cai, J. Liu, J. Su, L. Sun, S. Chen, J. Xia, J. B. King, "Behavioral Model for RF Power Transistors Based on Canonical Section-Wise Piecewise Linear Functions," *IEEE Trans. Microw. Theory Techni.*, vol. 68, no. 4, pp. 1409-1422, Apr. 2020.

[3] E. M. Azad, J. J. Bell, R. Quaglia, J. J. M. Rubio, and P. J. Tasker, "New Formulation of Cardiff Behavioral Model Including DC Bias Voltage Dependence," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 607-610, June 2022.

[4] X. Tang, A. Raffo, N. Donato, G. Crupi and J. Cai, "Theoretical and Experimental Analysis of a CSWPL Behavioral Model for Microwave GaN Transistors Including DC Bias Voltages," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 43, no. 3, pp. 933-943, March 2024.