A 23-GHz Quadrature Switched Capacitor Power Amplifier

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***Abstract*—To meet the requirement of mm-wave communication systems including 6G and SATCOM with merits of high efficiency and linearity, this project investigates a mm-wave quadrature switched capacitor power amplifier (SCPA) that is necessary for such transmitters (TX). In this project, a 10-bit quadrature SCPA is presented and implemented. The differential LOs with the in-phase and quad-phase (i.e., LOI and LOQ signals) are generated by two identical couplers. The sign bits BBI⟨9⟩ and BBQ⟨9⟩ determine the quadrant of the output signals. Meanwhile, the quadrature SCPA is composed of 6-bit MSB and 3-bit LSB unit cells to amplifier the signals. Then, a differential to single-ended transformer with a capacitor is introduced at the output port. To verify the mechanism mentioned above, the proposed quadrature SCPA is simulated based on 40nm CMOS technology. The proposed SCPA exhibits 21.2-dBm peak output power (P_{out}) and 37.8% drain efficiency (DE) at 23 GHz.**

***Index Terms*—CMOS, mm-wave, switched capacitor power amplifier (SCPA), quadrature, transmitter (TX).**

I. Introduction

THE modern wireless communication systems in portable devices including 6G and SATCOM require transmitters (TXs) with high power efficiency and lower power consumption. The polar TXs [1], [2] are proposed with high peak efficiency. However, the polar TXs require a complex coordinate rotation digital computer (CORDIC) and phase modulator (PM). Besides, the phase control and amplitude control should be synchronized, which could affect bit error rate and error vector magnitude (EVM) performance. Compared to polar TXs, quadrature TXs [3], [4] show advantages of simpler architecture and higher data rate. Meanwhile, as one of the important components in TX, power amplifiers (PAs) have been widely investigated in recent years, especially the digital PAs which have merits of high efficiency and flexibility of operation modes [5], [6], [7]. The switching unit cells contribute to the high efficiency of digital PAs. Nevertheless, the quadrature SCPA operating at mm-wave still remains a great challenge. Thus, this project introduces a 10-bit SCPA that shows a high power efficiency and linearity, which is attractive for the application of mm-wave quadrature transmitter in 6G and SATCOM.

II. Circuit Design

Fig. 1 presents the architecture of the proposed quadrature SCPA, which consists of four sections: two identical couplers, a sign-map, a SCPA array using 6-bit MSB and 3-bit LSB quadrature unit cells, and a differential to single ended transformer. Firstly, the differential LO signals are injected in the same couplers and a sign-map to generate the quadrature signals, which are determined by the sign bit BBI⟨9⟩ and BBQ⟨9⟩. Then, the quadrature signals are amplified by the SCPA consisting of 6-bit MSB and 3-bit LSB with the control of baseband (i.e., BBI and BBQ) and four quad-phase signals (i.e., I+, I-, Q+, Q-). Finally, a differential to single-ended transformer with a capacitor is used to generate the output signals.

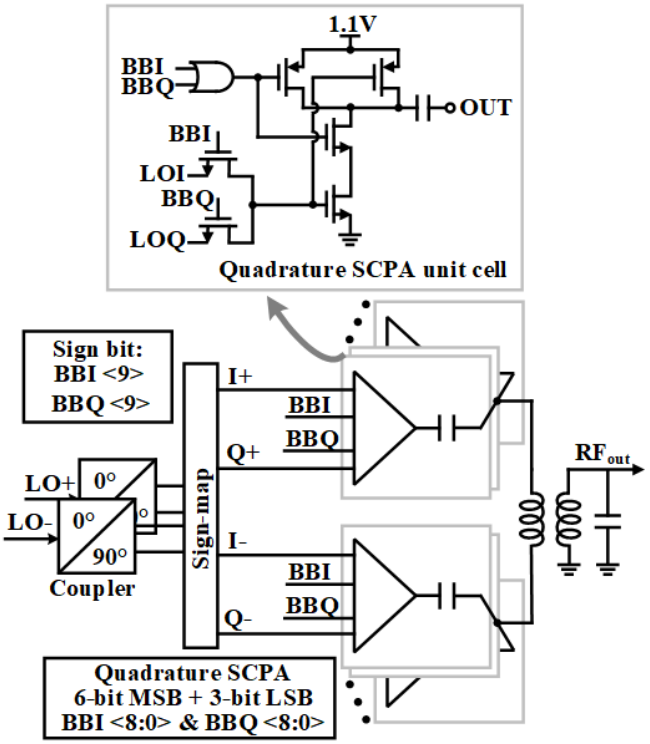

Fig. 1. The architecture of the proposed quadrature switched capacitor power amplifier.

A. Quadrature Signals Generation

Quadrature signals with low amplitude and phase imbalances are critical for SCPA design. Thus, the passive coupler is designed to achieve 90° phase difference with high isolation between output ports and within a wide operation frequency band. Then, the differential LOs with the in-phase and quad-phase (i.e., I and Q signals) are generated by aforementioned two identical couplers. Here, the quadrant of output signals is selected by the sign-map circuit that simultaneously controlled by sign bits BBI⟨9⟩ and BBQ⟨9⟩.

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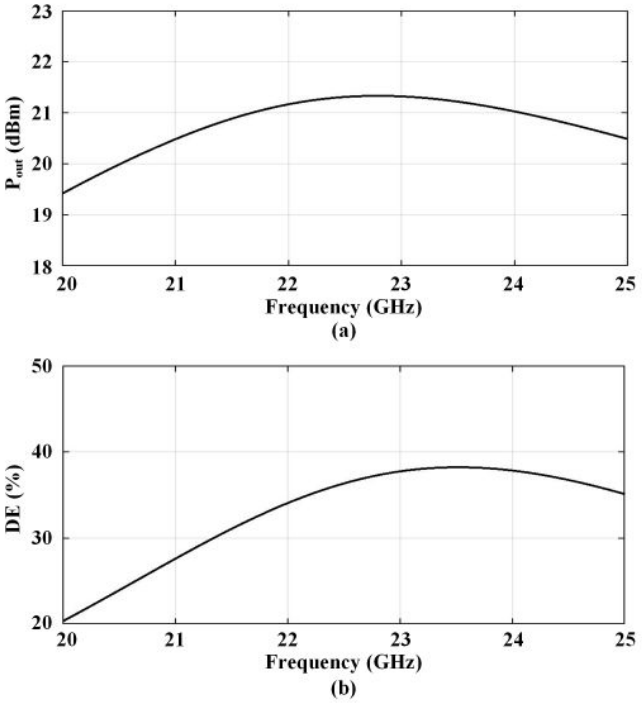

Fig. 2. Simulated (a) saturated output power P_{out} and (b) DE of SCPA.

B. SCPA array

The SCPA array is consists of 6-bit MSB and 3-bit LSB unit cells. The circuit of each unit cell is shown in Fig. 1. The sizes of the NMOS transistors are 40 um/40 nm, while the sizes of PMOS transistors are 20 um/40 nm. The capacitor is 32fF for the 6-bit MSB unit cell. The unit capacitors for the 3-bit LSB unit cell capacitors are 16, 8, and 4fF, which can be achieved in the CMOS technology. The voltage supply of NMOS transistors is 1.1 V. BBI and BBQ are BB control signals for in-phase and quad-phase, respectively. Here, the BBI and BBQ cannot be 1 at the same time. Then, the amplified signal are output by a differential to single-ended transformer.

III. Result

The proposed quadrature SCPA was simulated in 40nm CMOS technology. Fig. 2(a) and (b) depict the simulated saturated output power P_{out} and DE, repectively. It is found that the peak output power P_{out} is 21.2-dBm at 23 GHz, while the drain efficiency DE is 37.8% at 23 GHz. The voltage supply is 1.1 V. Table I summarizes and compares major performances with prior-art mm-wave mixed-signal PAs.

IV. Conclusion

In this project, a 10-bit quadrature switched capacitor power amplifier (SCPA) is presented for mm-wave transmitter application in 6G and SATCOM. Passive coupler and sign-map controlled by sign bits are utilized for quadrature signals generation. Meanwhile, 6-bit MSB and 3-bit LSB SCPA array with a differential to single-ended transformer is employed to amplifier and output the signals. Based on 40nm CMOS process, the proposed SCPA is implemented with 21.2-dBm peak output power P_{out} and 37.8% drain efficiency DE at 23 GHz.

TABLE I
Performance Summary and Comparison

Reference	**This Work***	[1]	[3]	[5]
Technology	**40nm CMOS**	40nm CMOS	40nm CMOS	22nm CMOS FOI
Architecture	**Quadrature I/Q sharing SCPA**	Four-way series Doherty	Double-quadrature direct upconverter with series Doherty balanced PA	Edge combining class D
Fre. (GHz)	**23**	29.5	27	28
Supply (V)	**1.1**	1	1	0.9/1.8
P_{out} **(dBm)**	**21.2**	18.7	20	21.2
DE (%)	**37.8**	24	28.5	22.1

*: simulated results.

V. Acknowledgment and Next Plan

I am extremely grateful to the IEEE MTT-Society Undergraduate/Pre-graduate Scholarship for motivating and supporting me to take up research in the wireless circuit field. I also want to thank my supervisor Professor Xun Luo for his guidance on radio-frequency integrated circuits (RFIC) design. After the graduation of bachelor, I will continue pursuing the Ph.D degree in areas of wideband microwave/mm-wave integrated circuits, especially the mixed-signal transmitter with its circuit modules, e.g., power amplifier, etc, in University of Electronic Science and Technology of China. I will continue to accumulate experience to become a RFIC designer and fix my next plan to make further progress in providing efficient communication for humanity.

References

[1] M. Mortazavi *et al.*, "A four-way series Doherty digital polar transmitter at mm-wave frequencies," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 803–817, Mar. 2022.
[2] S. Zheng *et al.*, "A CMOS WCDMA/WLAN digital polar transmitter with AM replica feedback linearization," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1701–1709, Jul. 2013.
[3] M. Pashaeifar *et al.*, "A millimeter-wave mutual-coupling-resilient double-quadrature transmitter for 5G applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3784–3798, Dec. 2021.
[4] B. Yang *et al.*, "Millimeter-wave quadrature mixed-mode transmitter with distributed parasitic canceling and LO leakage self-suppression," *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 691–704, Mar. 2023.
[5] H. M. Nguyen *et al.*, "A mm-wave switched-capacitor RFDAC," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1224–1238, Apr. 2022.
[6] Z. Deng *et al.*, "A dual-band digital-WiFi 802.11a/b/g/n transmitter SoC with digital I/Q combining and diamond profile mapping for compact die area and improved efficiency in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 172–173.
[7] Y. Yin *et al.*, "A broadband switched-transformer digital power amplifier for deep back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2997–3008, Nov. 2020.