Heterogeneous Integration of GaN and Si for MMICs above 300 GHz, 6G Applications and Beyond

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***Abstract*— With data rates pushing into the Tbps, there is an urgent need for the use of mmWave and sub-terahertz RF front ends and transistors. Gallium Nitride (GaN) transistors have continued to push the limits of high-power density, high frequency semiconductor devices. The future of GaN radio frequency (RF) circuit technology is at the intersection of device engineering, advanced packaging, and circuit design. To design the most efficient W-G Band devices and systems, we must embrace a design/system-technology co-optimization (DTCO/STCO) approach, that combines innovative GaN transistors with engineered linearity, novel heterogeneous integration with state-of-the-art Silicon (Si) bias and control circuitry, and advanced physics-based modeling. This report lays the foundations of a single-chip 3D-stacked radio frequency (RF) Front End module.**

***Index Terms*—3DIC, 3DHI, DTCO, STCO, III-V, GaN FEOL, Si CMOS BEOL.**

I. INTRODUCTION

ENERGY consumption of the world's communication networks exceeds 1% of the global energy production and it is increasing exponentially. In addition, by 2040 the amount of generated data will be at least 20× larger than what can be transmitted through this network. These two trends will dramatically change communication systems in the future. To truly revolutionize wireless chip design, we must adopt a multi-substrate, single-chip 3DIC approach.

With the introduction of 3D-stacked GaN dielets to silicon control circuits, the efficiency of RF subsystems can be increased dramatically. Chiplet level integration of GaN transistors has occurred using wire bonds for switching applications [1]. Wire bonds are an excellent choice for frequency ranges up to megahertz, but are quite lossy at higher frequencies, especially in the sub-terahertz regime. Integration has also occurred at the monolithic level. This method demonstrates regrowth of GaN on a Si CMOS substrate, allowing for GaN and Si devices to be situated on the same substrate in close vicinity. The issue here lies in the uniformity of the fabricated devices. The Si devices are far more reliable and uniform in performance than the regrown GaN devices are, resulting in an overall reduction in yield. Wafer level bonding has also been explored, with Si CMOS devices being bonded onto a GaN substrate [2]. While previous 2D III-V back-end-of-line (BEOL) chiplet-level schemes have been presented for the heterogeneous integration of Gallium Nitride [3], the need for dielet-level 3DHI leveraging Si CMOS BEOL and FEOL is required for cost-effective, small footprint, high performance 3DIC circuits. This integration will be possible through highly scaled CMOS compatible interconnects and novel, 3D-stacked advanced packaging. The goal of this approach is to have Si-based bias, passive and digital circuitry directly control custom-placed GaN high electron mobility transistor (HEMT) dielets, with localized, embedded glass in a compact, vertically stacked, single package solution, as shown in Fig. 1.

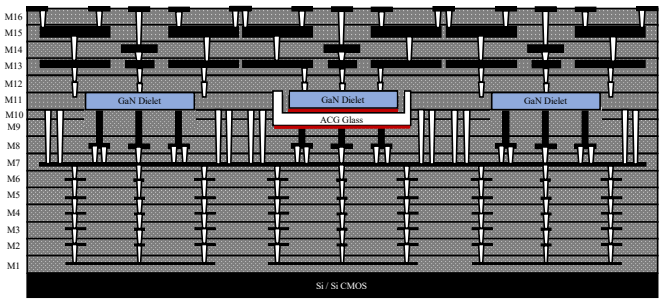

Fig. 1. Bespoke single chip 3DIC "vision" with multiple GaN dielets leveraging Si BEOL and embedded glass for passives

II. ALGAN / GAN-ON-SI/ENGINEERED SUBSTRATE HEMTS

Gallium nitride-based HEMTs currently define the state-of-the-art in high power density, high frequency semiconductor devices. The first demonstration of an RF HEMT fabricated using engineered substrate (GaN-on-QST®) is presented [4]. The epitaxial structure of the engineered substrate used in this work is shown in Fig. 2(a). In addition, a W-Band GaN-on-Si RF HEMT is also fabricated. In the first step, the source and drain were formed using Ti (20 nm)/Al (100 nm)/Ni (25 nm)/Au (50 nm) metal stack and lift-off process, then alloyed at 825 °C in N_2 ambient for 30 seconds. Device isolation was established via a mesa using BCl_3/Cl_2 plasma reactive ion etching (RIE). Lastly, a T-gate structure was fabricated using a polymethyl methacrylate (PMMA)-based bi-layer stack and electron beam lithography. A T-gate structure was chosen to decrease the gate resistance, thereby allowing for higher power gain. A Ni (30 nm)/Au (310 nm)/Ni (30 nm) metal stack was evaporated to form the T-gate for the GaN-on-Engineered HEMT, while a more aggressive Ni (30 nm)/Au (450 nm)/Ni (30 nm) metal stack was used for the GaN-on-Si HEMT. The reported GaN-on-Engineered HEMT featured a source-to-drain distance, L_{SD}, of 520 nm and a gate length, L_G, of 200 nm. The GaN-on-Si HEMT featured a source-to-drain distance, L_{SD}, of 575 nm and a highly scaled gate length, L_G, of 120 nm.

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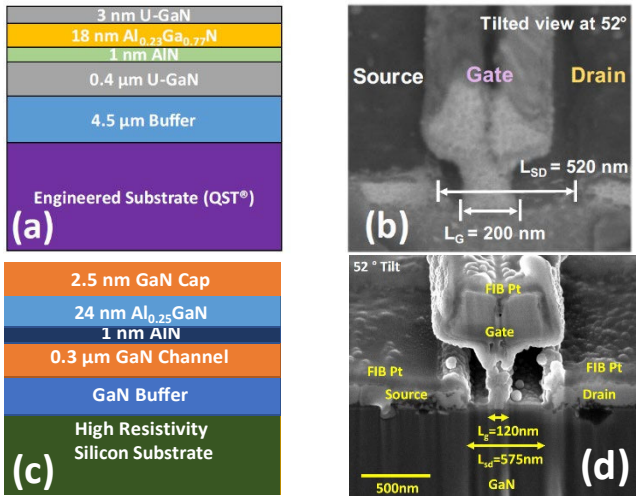

Fig. 2. (a) AlGaN/GaN epitaxial structure on engineered substrate (QST®). (b) Cross-section of a fabricated transistor, showing L_{SD}=520 nm, L_G=200 nm. (a) AlGaN/GaN epitaxial structure on Silicon. (b) Cross-section of a fabricated transistor, showing L_{SD}=575 nm, L_G=120 nm.

The RF small-signal performance of the HEMTs was characterized from 100 MHz to 40 GHz by using an Agilent N5230A vector network analyzer. As seen in Fig. 3(a), an f_T /f_{max} of 48/115 GHz was achieved (without de-embedding) for GaN-on-Engineered Substrate and an f_T /f_{max} of 95/173 GHz was achieved (with de-embedding) for GaN-on-Si. Further work is being conducted to have a direct comparison between Engineered substrate and silicon.

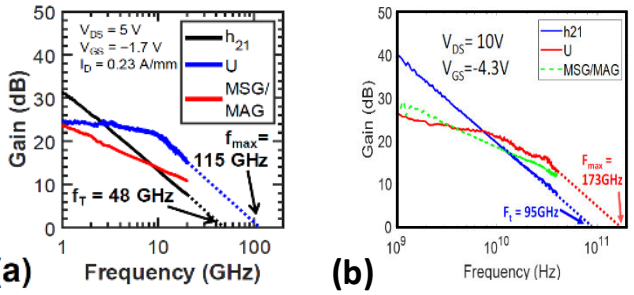

Fig. 2. (a) Small signal characteristic of GaN-on-QST (without de-embedding). (b Small signal characteristic of GaN-on-Si (with de-embedding).

Stealth dicing is used to produce dielets from the 200mm wafer or piece to sizes of 200µm x 400 µm.

III. Si CMOS Back-End-Of-Line Tapeouts

At higher frequency signals, especially at sub-Thz frequencies, the parasitic capacitance between the gate and the drain of the GaN FEOL device becomes quite problematic. To circumvent this problem, a neutralization capacitance between the alternate drain and gate of a differential pair of transistors can be used to increase the power gain, stability, and reverse isolation. The neutralization capacitance of the fabricated GaN HEMT - found to be 3 fF, biasing, and matching of the GaN FEOL was implemented in Si CMOS BEOL. The Si CMOS BEOL was completed in Intel16 22nm FinFET PDK, as seen in Fig. 10. The GaN FEOL was modeled using the MIT Virtual Source GaN Model and simulated to target 20-50GHz with 10dB of stable gain. Co-simulation was completed in HFSS for electromagnetic simulation, ADS for RF system level simulations, and Cadence for chip layout/transient simulations.

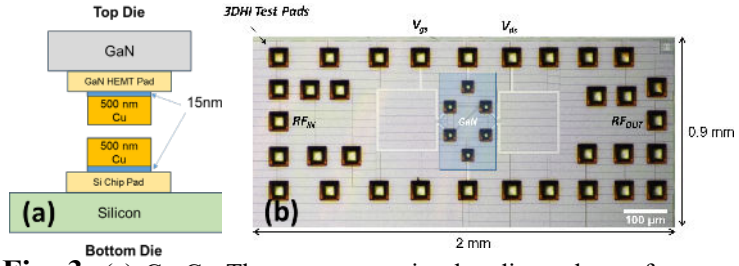

Fig. 3. (a) Cu-Cu Thermocompressive bonding scheme for GaN dielet integration with Si CMOS BEOL Circuit. (b) Si CMOS BEOL chip micrography.

The Si CMOS BEOL chip is integrated with the highly scaled mmWave GaN dielet using fine pitch copper pillar thermocompressive bonding. A formic acid module is used to prevent oxidation between the bond and low bonding temperature is key (<400°C) to mitigate degradation to the Si CMOS chip. The copper pillars have diameters of 25 µm and 35 µm for the GaN pads and Si CMOS pads, respectively. This mismatch is size not only allows for added alignment tolerance but also the potential for hybrid bonding incorporating oxide in the future.

IV. Fellowship Impact and Career Plans

I am extremely grateful for the IEEE Microwave Theory and Technique Society (MTT-S) for bestowing upon me this fellowship and supporting my research on the next generation of RF circuits. Attending IMS 2023 brought upon fond memories of my first IMS and a power amplifier design competition that would shape my career, in Boston 2019. It was great to meet old friends and mentors again. I hope to revolutionize the fields of microwaves and THz chip design from devices to circuits, whether it is through industry, academia, or perhaps even my own venture.

References

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