A Multi-Purpose Baseband Signal Generator System for Digital PMCW D-Band Radars in 22nm FDSOI

Florian Probst, *Graduate Student Member, IEEE,* and Robert Weigel, *Fellow, IEEE.*

***Abstract*—This report proposes a multi-purpose baseband signal generator system for phase-modulated continuous-wave (PMCW) radar transmitters. It combines a divide-by-five clock divider, a controllable delay circuit, and an in-operation configurable linear-feedback shift register (LFSR)-based pseudo-random binary sequence (PRBS) generator that can be evaluated separately. The system enables the orthogonalization of transmit channels in the range and code domain, and its sub-blocks are implemented with custom true single-phase-clock (TSPC) flip-flops. Realized in a 22 nm fully-depleted silicon on insulator (FDSOI) technology, the fabricated IC can generate alternating, delayable PRBSs up to a maximum bit rate of 27 Gb/s.**

***Index Terms*—Digitally modulated radars, FDSOI, PMCW radar, PRBS generator.**

I. Introduction

State-of-the-art CMOS technology enables radar systems at millimeter-wave (mm-wave) frequencies, such as the D-band, which provide increased bandwidth and, thus, a better range resolution. The so-called PMCW radar uses an alternative waveform to the widespread frequency-modulated continuous-wave (FMCW), where a PRBS is binary phase-shift keying (BPSK) modulated onto a fixed carrier frequency. The receive signal is down-converted and digitized, followed by a DSP that includes a correlation with the modulated PRBS, as shown in Fig. 1. Apart from giving the range profile, the modulation sequence can be used for separation between channels in MIMO or joint radar communication (RadCom) systems [2]. Since the system's range resolution depends on the data rate of the PRBS, it must be chosen accordingly, making its generation a challenging research problem.

In the proposed project, different PRBS generators for the application in an integrated 140 GHz PMCW radar transmitter are investigated and realized on a 22 nm FDSOI technology. The radar system shall be used for gesture recognition, enabling non-contact human-machine interaction, e.g., in smartphones or car entertainment systems.

Generally, two possibilities exist to generate pseudo-noise sequences. One uses an LFSR of N_{FF} flip-flops (FFs) with XOR feedback. It can generate m-sequences of length $2^{N_{\mathrm{FF}}}-1$ and is most efficient regarding area and power consumption, which we previously proposed in [1], [3], and integrated into an overall PMCW radar transmitter in [4]. LFSRs' main disadvantage is the limited flexibility in sequence choice, meaning that more advanced sequence families like the almost perfect auto-correlation sequence (APAS) cannot be utilized, and interference between radar systems that use the same modulation signal can occur. Therefore, an alternative generator incorporating a programmable digital shift register connected to a high-speed serializer was proposed in [5]. The circuit features a clock divider that provides a divided digital clock, built from standard cell (SC) elements from a foundry-provided library, which proved to be the bottleneck regarding the achievable maximum bit rate.

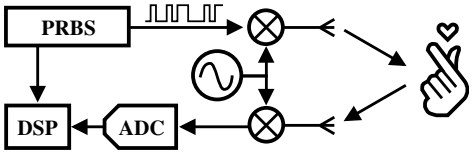

Fig. 1. Simplified block diagram of a PMCW radar system [5].

Below, we propose a multi-purpose baseband generator system offering solutions for multiple problems that occurred during the design and evaluation of the above designs.

II. Project Outcome

Fig 2 shows the block diagram of the proposed generator system, which tackles the following problems:

1) As the employed SC-based divider is the limiting factor for the maximum achievable data rate of the arbitrary sequence generator, an alternative divider topology based on TSPCs FFs is adopted to outperform the SC version.
2) A disadvantage of PMCW radar is the necessity of high-speed analog-to-digital converters (ADCs) in the receiver. An analog correlator can solve this problem by reducing the required sampling rate. The approach requires time-delayed modulation signals [6], so the proposed system includes a delay circuit postponing the generator start that also enables MIMO systems based on range domain orthogonalization.
3) Simulation results suggest using an advanced modulation frame that reduces the range sidelobes arising from Doppler shift [7]. However, the alternative modulation signal incorporates multiple different m-sequences in a radar frame and, consequently, cannot be generated by a conventional LFSR. Therefore, an advanced LFSR with programmable feedback taps is included, which also enables sequence orthogonalization.

The interested reader is referred to the respective publications of the divider [8] and the programmable LFSR [9] for their circuit design and measurement results. Therefore, we

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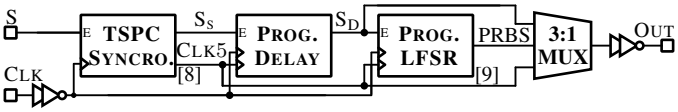

Fig. 2. Block diagram of the proposed generator system including a divider by five, a delay circuit, and a programmable LFSR.

can focus on the implementation and measurement of the delay circuit.

As anticipated by Fig. 2, the delay is generated by delaying the signal S_S starting the LFSR. This approach reduces the required design effort, as only a falling edge must be postponed, which can be partially executed in the digital domain by a programmable counter. It generates the coarse delay, a multiple of five of the input clock's period, which must then be finely delayed, conducted by a shift register of TSPC FFs. The outputs of five FFs are connected to a three-stage-inverter-based multiplexer, resulting in the schematic shown in Fig. 3.

Multiple oscilloscope snapshots are generated, and their relative time delay is evaluated to show the feasibility of the delay circuit in a measurement. An arbitrary waveform generator (AWG) generates a rectangular signal, which is split and connected to the start input of the integrated circuit (IC) and the oscilloscope's external trigger input. The baseband system's output multiplexer connects the LFSR to the output buffer, so the measurement shows a PRBS signal. Fig. 4 shows the time-domain measurement result at a data rate of 20 Gb/s for different delay configurations in the top graph and the corresponding correlation result with the expected m-sequence underneath. The delay circuit's correct operation is reflected in the uniform delay applied to the first falling edge of the PRBS, as well as the shift of the correlation peaks, representing a sequence repetition. At an input clock frequency of 20 GHz and a supply voltage of 0.8 V, the delay FFs exhibit a power consumption of 0.44 mW. When all functionality is enabled, including the LFSR, the system consumes 12 mW.

To the author's knowledge, no comparable circuit that operates at these data rates is presented in the literature. In particular, at the aimed range resolution, it enables cost-effective receiver systems that do not require a complex DSP. Furthermore, using the shown delay options 0, 512, 1024, and 1536, a MIMO system with four transmit channels orthogonalized in the range domain can be implemented.

III. Fellowship Impact and Career Plan

I am deeply grateful to the IEEE MTT-S for awarding me the prestigious MTT-S Graduate Fellowship in 2023, which

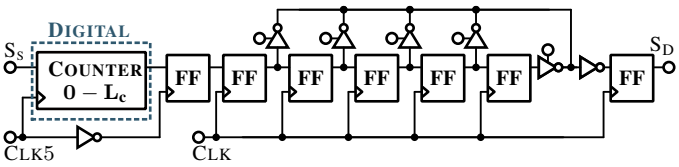

Fig. 3. Hardware realization of the delay circuit.

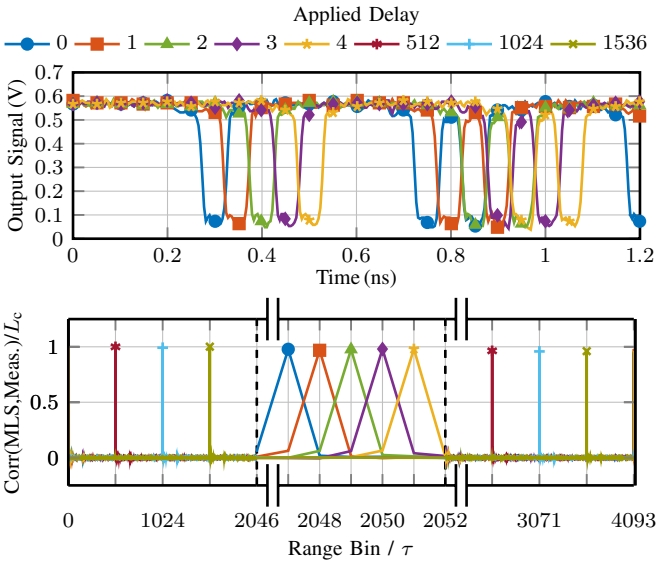

Fig. 4. Time domain measurements for different delay configurations on top and the corresponding correlation result with the expected m-sequence on the bottom.

significantly supported my research. The fellowship allowed me to attend the 2023 International Microwave Symposium (IMS) in San Diego, CA, a highly valuable experience which provided a fantastic opportunity to network with global experts and gain insights into cutting-edge research. The industrial exhibition was particularly enlightening, showcasing the latest developments and products firsthand. My immediate goal is to complete my Ph.D. in integrated mixed-signal circuit design, followed by a career focused on technical innovation. I strongly encourage all eligible graduate students in the microwave field to apply for the MTT-S Graduate Fellowship.

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