A Heterogeneous Mode-Converting Power Radiator for Broadband Sub-THz Applications

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***Abstract*—In this report, we briefly summarize the progress of the 2023 MTT fellowship awarded project. In this work, we propose the design of a broadband heterogenous mode-converting power radiator for above 100 GHz frequencies. The power amplifier employs a new topology to improve interstage matching and utilizes a novel 8-to-1 combiner to increase the output power level. Furthermore, we present chip-to-PCB interface circuitry along with the broadband antenna design.**

***Index Terms*—power amplifier, wirebond, antenna, beyond 5G.**

I. Introduction

In the realm of sub-THz communication systems, there has been a visible rise in interest due to their potential for substantially enhanced data rates relative to traditional technologies such as 5G cellular mobile systems. To meet the escalating demand for increased data rates, the frequencies of operation of beyond-5G transmitters and receivers are being extended beyond the 100 GHz threshold, capitalizing on the availability of ample bandwidth resources.

When designing a broadband transmitter circuit, significant challenges emerge with the power amplifier (PA) and antenna exerting the most pronounced influence on gain and bandwidth performance. Notably, frequencies exceeding 100 GHz pose limitations on devices like complementary metal oxide semiconductor (CMOS) or Silicon-Germanium (SiGe) in generating sufficient output power, exacerbating the already high path loss within this frequency band and increasing the difficulty of high-power transmission. Consequently, achieving higher power levels necessitates high-gain PAs and antennas. While on-chip antennas offer system-level integration advantages, they often lack adequate gain and bandwidth. In contrast, PCB/FPC antennas, as demonstrated in [1]- [3] afford superior gain and bandwidth. Furthermore, the gain of antennas can be augmented through the design of large antenna arrays, particularly advantageous given the cost-effectiveness of implementing PCB antennas. Should off-chip antennas be chosen for their superior performance, careful integration of the interface between the chip and antenna with the rest of the circuitry is essential. However, existing flip-chip technologies like copper pillars and solder bumps fail to meet the demands of broadband sub-THz signal transmission. Consequently, novel broadband and low-loss interface technologies tailored to this frequency range are imperative.

In this work, we propose an 8-way broadband power amplifier, a low-loss broadband chip to PCB interface, and a broadband dual-polarized off-chip antenna. A comparison of on-chip and off-chip antennas along with the proposed offchip antenna design are presented in Section II. The interface between chip and PCB is discussed in Section II along with the proposed low-loss broadband chip-to-FPC interface. In Section III, we review some state-of-the-art PA combiners and propose a broadband 8-way power combiner. Finally, the career plan and fellowship impact is provided in Section IV.

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II. Elements of a high Power sub-THz Radiator

A. Antenna elements

In the conventional patch antenna, a narrow feedline is connected to a wider patch which results in narrowband impedance matching. On the other hand, the aperture-coupled stacked patch antenna (ACSP) employs a narrow slot for interfacing with the feedline. In [2], authors demonstrate that by designing a two-section feedline, and choosing its length and characteristic impedance judiciously, a broadband matching between feedline and slot is achieved. Furthermore, to attain a considerable level of gain across broadband frequencies, two metal layers are employed for designing the patches. The broadband matching between the slot and patches is achieved by optimizing their vertical coupling, ensuring that the impedance of the slot and patches are within the acceptable voltage standing wave ratio (VSWR) level. At mm-wave frequencies, the feedline induces the parallel plate mode in the transverse direction to the propagating wave in the feedline which leads to the gain drop. This phenomenon is mitigated by incorporating vias around the feedline. Similarly, the parallel plate mode generated by the patches causes a decrease in antenna gain. To address this, in [1], authors proposed a cavity-backed antenna aiming to suppress the parallel plate mode around the patches. Fig. 1(a,b) illustrate the three-dimensional and detailed planar schematic view of the antenna, respectively. As shown in Fig. 1(c) the antenna achieves a measured peak gain of 8.1 dB and covers 91.5-134 GHz. Future endeavors aim to integrate two such antennas which are fed orthogonally to extend bandwidth and also create dual-polarizaed radiation.

B. Interface Design

The offchip antenna offers superior gain and significantly wider bandwidth in comparison to on-chip counterparts. However, the primary limitation lies in the interface between the chip and PCB. Recently, in [4], the authors have proposed a wire-bond interface between the chip and PCB specifically for Frequency Modulated Continuous Wave (FMCW) radar

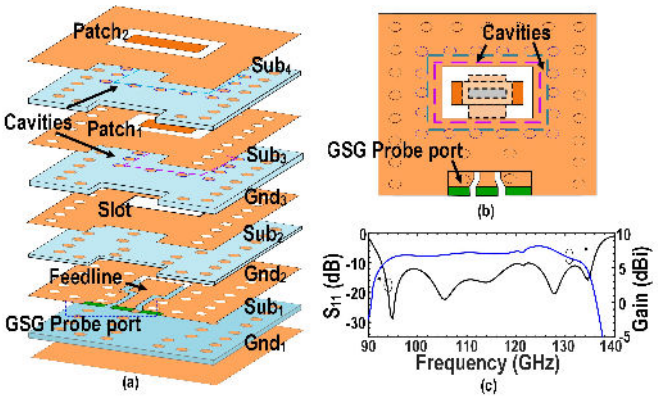

Fig. 1. (a) Proposed broadband antenna, (b) the designated cavities help with the surface wave cancellation, and (c) gain and S_{11} plots.

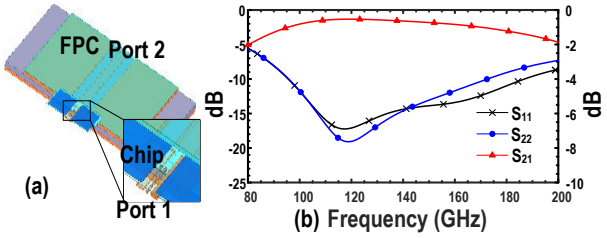

Fig. 2. (a) Proposed interface design, (b) S-parameter results

applications at 60 GHz. The additional inductance introduced by the wirebond is compensated at the PCB side by incorporating transmission line stubs. To minimize the insertion loss, a novel mode converter interface has been introduced where a grounded co-planar waveguide (GCPW) transmission line is utilized and the electric field propagates along a slot oriented in the transverse direction. This slot field is coupled to the transmission line employed at the PCB layer as shown in Fig. 2(a). As depicted in Fig. 2(b), the 10 dB input and output matching span from 95.7 to 172.5 GHz and 95.7 to 186.7 GHz, respectively. The insertion losses fall within the range of -0.52 to -1.4 dB. However, the addition of a thicker interface layer between the chip and PCB increases the insertion loss. It is to be noted that the field in the slotted line is bound and results in a tighter coupling with the PCB. To reduce the insertion loss, the slot is required to radiate the field which is currently under evaluation by authors.

III. Broadband Power Amplifier Design

Designing a broadband power amplifier (PA) poses various challenges. The maximum frequency of unilateral power gain (f_{max}) defined as $f_{max} = \sqrt{f_t/8\pi R_g C_{gd}}$, where $f_t = g_m/2\pi(C_{gs}+C_{gd})$ impacts the power amplification capabilities of the transistors. While a larger device size delivers greater current and thus higher power levels, the associated parasitics also increase. Notably, parasitics such as gate-to-drain and gate-to-source capacitances (C_{gs} and C_{gd}) and gate resistance (R_g) substantially reduce f_{max}, limiting the utility of larger devices. To enhance power levels, numerous PAs utilize smaller devices combined in parallel through a power combiner [5]. For broadband PAs, the combiner

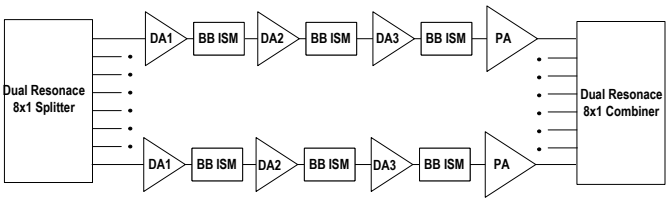

Fig. 3. Proposed broadband PA with input splitter and out combiner

must also be broadband; however, the device's input and output impedance, typically with small magnitude and negative imaginary part (capacitive), pose challenges for broadband impedance matching. Although transformer-based interstage matching is commonly employed, its limited self-resonance frequency (SRF) restricts its application in PA designs above 100 GHz. In the proposed design, we address these challenges to realize a broadband PA. The author has completed the simulation, and awaiting the chip fabrication followed by the measurement.

IV. Career Plan and Fellowship Impact

The authors would like to extend their gratitude to the IEEE Microwave Theory and Technique Society (MTT-S) for this fellowship award. This esteemed recognition has served as a significant source of motivation, inspiring the author to persist in his research endeavors in the field of millimeter-wave integrated circuit (IC) design. With this honor fueling his determination, the author is eager to progress with the planned fabrication efforts in the forthcoming months, as well as to delve deeper into various research challenges within the millimeter-wave domain. Upon successful realization of this project, the author would like to pursue more research projects in academia or industrial research institutions.

Acknowledgments

The authors would like to thank IEEE MTTS for their support of this project through the graduate fellowship award. We would like to also thank National Science Foundations and MFLEX Inc. for their support of our project and fabrication of the antennas, respectively.

References

[1] M. H. Maktoomi, S. Saadat, O. Momeni, P. Heydari and H. Aghasi, "Broadband Antenna Design for Terahertz Communication Systems," *IEEE Access*, vol. 11, pp. 20897-20911, 2023.

[2] M. H. Maktoomi, Z. Wang, H. Wang, S. Saadat, P. Heydari and H. Aghasi, "A Sub-Terahertz Wideband Stacked-Patch Antenna on a Flexible Printed Circuit for 6G Applications," *IEEE Transactions on Antennas and Propagation*, vol. 70, no. 11, pp. 10047-10061, Nov. 2022.

[3] M. H. Maktoomi, Z. Wang, H. Wang, S. Saadat, P. Heydari and H. Aghasi, "A GSG-Excited Ultra-Wideband 103–147 GHz Stacked Patch Antenna on Flexible Printed Circuit," *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (APS/URSI)*, Singapore, Singapore, 2021, pp. 1829-1830.

[4] X. Liu, M. H. Maktoomi, M. Alesheikh, P. Heydari and H. Aghasi, "A 49-63 GHz Phase-locked FMCW Radar Transceiver for High Resolution Applications," *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, Lisbon, Portugal, 2023, pp. 509-512.

[5] D. Zhao and P. Reynaert, "An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 683-690, Feb. 2015