Design of An Impedance Transforming Circulator in 130nm CMOS

Kaustubh Pabba, *Student Member, IEEE,* Imon Mondal, *Member, IEEE*

***Abstract*—This project report describes an impedance-transforming circulator (ITC) designed and simulated in 130nm CMOS for 1GHz operation. The inherent impedance transforming ability of quarter-wave transmission lines is exploited in the circulator core to facilitate efficient co-design of circulator-PA-LNA transceiver architecture. The designed circulator incorporates clock-boosting in the gyrator section clocking to improve linearity by avoiding the possibility of false switching. The simulated TX-ANT/ANT-RX transmission losses at the frequency of operation are 3.3dB and 4.5dB, respectively. The circulator achieves a simulated TX-RX isolation of 25dB across 100MHz BW centered at 1GHz while consuming 48mW DC power.**

***Index Terms*—Circulators, CMOS, full-duplex (FD), non-reciprocity, clock boosting, impedance transformation, impedance transforming circulator (ITC).**

I. Introduction

Fully Duplex (FD) wireless systems constitute a wide range of systems that can transmit and receive simultaneously and at the same frequency. Such systems possess twice the network capacity at the physical layer. Subsequently, FD systems would enable the realization of higher data standards, and possibly higher link ranges with the utilization of relays/repeaters. One of the fundamental hurdles in realizing such systems is the conception of the antenna interface. The approaches taken in the past have had their fair share of issues as follows: CMOS incompatibility due to the usage of magnetic components, higher form factor, and having a fixed minimum fundamental loss. Recently, non-reciprocal magnet-free circulators were demonstrated by exploiting time variance, making such implementations automatically viable for integration into CMOS systems. However, in these existing architectures [1], [2], and [3], the power amplifier (PA) at the TX port, and the Low Noise Amplifier (LNA) at the RX port, are conditioned to be functioning in a 50Ω interface, i.e., by having an impedance equivalent to that of the antenna. Such design choices translate into sub-optimal PA efficiency and RX Noise Figure (NF), which are critical aspects related to the design of an RF transceiver.

With the incentive to leverage the full potential of the circulator, this project proposes an architecture that exploits the inbuilt impedance transforming ability of quarter wave transmission lines to facilitate the efficient co-design of circulator-PA-LNA transceiver architecture. This impedance-transforming circulator is designed in 130nm CMOS and operates at 1GHz.

K. Pabba was with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, UP, 208016, India.

K. Pabba is now with the Department of Electrical Engineering, Columbia University in the City of New York, New York, NY, 10027, USA.

I. Mondal is with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, UP, 208016. India

II. Working Principle

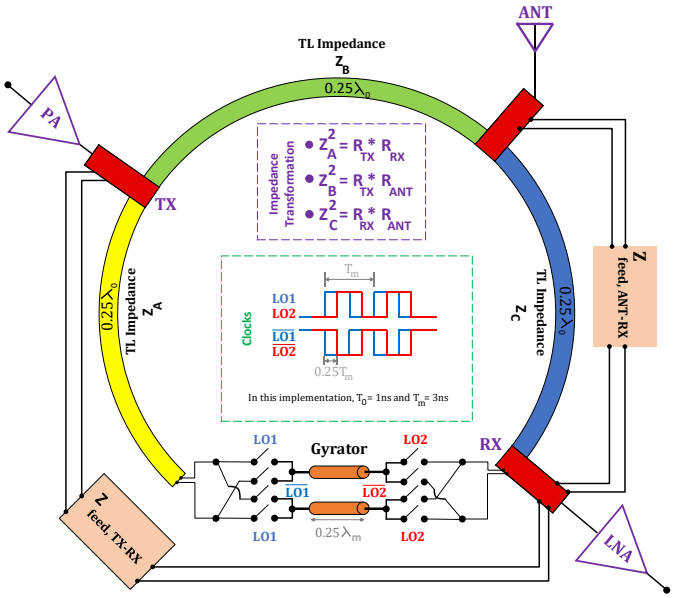

Fig. 1. Impedance Transforming Circulator Concept

Fig. 1 shows the conceptualized circulator facilitating impedance transformation. The quarter-wave transmission lines are designed to match both ends to their corresponding impedances. To build the circulator, a $3\lambda/4$ ring is wrapped around a non-reciprocal section called as the gyrator, which consists of a transmission line sandwiched between two sets of transistor switches, whose clocks are phase shifted with respect to each other. This gyrator element provides a non-reciprocal phase shift of 180° between the forward and reverse directions across a theoretically infinite BW. Such a condition is observed when the transmission line delay and clock phase shifts are given by $T_m = m \times T_0/4$, where m is the modulation index and T_0 is the period of the fundamental signal passing through the circulator. For modulation indices taking the form of odd integers, the circulator core and the gyrator provide phase shifts of (-270°, -90°) and (-270°, +90°) for waves traveling from each port in the clockwise (CW) and anti-clockwise (ACW) direction respectively. Consequently, waves end up canceling themselves in the ACW direction, lending to the sustenance of waves in the CW direction.

III. Design Choices & Simulation Results

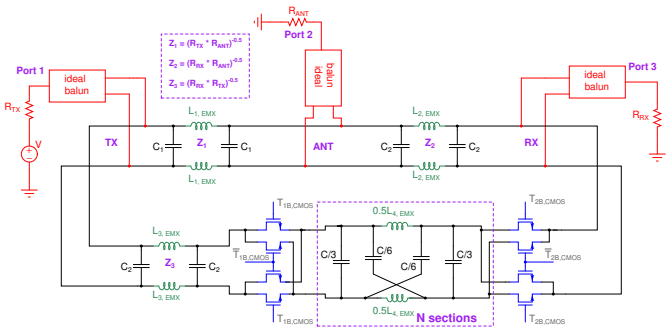

Fig. 2. Impedance Transforming Circulator Schematic

Fig. 2 shows the circuit schematic of the impedance-transforming circulator in differential mode. As shown, the $\lambda/4$ transmission lines have impedances ensuring matching on both ends of each line. Π-type CLC sections with a finite bragg frequency (ω_B) are used as lumped approximations for the transmission lines in the circulator core. Using the same CLC model for the gyrator transmission line gives higher losses as the switches act like frequency mixers, splitting the input power to different harmonics. To facilitate minimum power loss, one must design the line by ensuring its ω_B is as high as possible. Hence, a hybrid Π-CLC section is used to design the gyrator transmission line as it has a higher ω_B when compared to the Π-type CLC model. EMX-simulated differential spiral inductors with an octagonal geometry are used in the CLC sections that approximate the transmission lines.

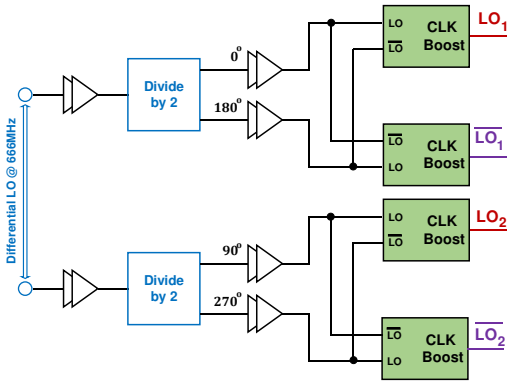

Fig. 3. Clock-Boosting Concept

A modulation index of 3 is assumed to design this 1GHz circulator, which requires the gyrator clocks to operate at 0.333GHz. For high enough TX power and limited clock swing, the transistor switches on the left end of the gyrator can undergo false switching. A clock-boosting mechanism is incorporated into the clocking circuitry to avoid the non-linearities induced by this false switching phenomenon. This mechanism helps in boosting the swing from V_{DD} to $3V_{DD}$ by shifting the high and low of a 0-V_{DD} signal by +V_{DD} and -V_{DD} each. A capacitive-based level shifting circuitry, as shown in Fig. 3, is used to shift the levels and is similar to the circuit described in [3].

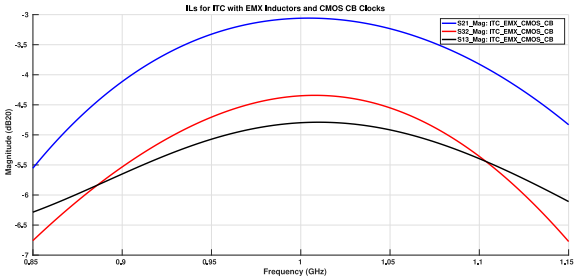

Fig. 4. Simulated Insertion Losses

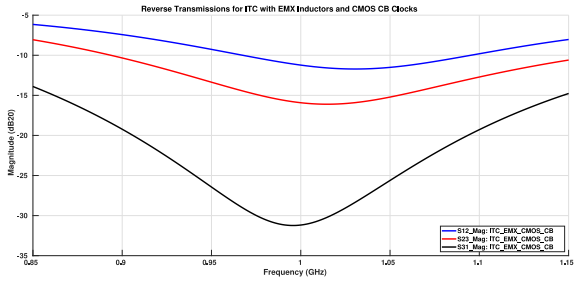

Fig. 5. Simulated Reverse Transmission Losses

IV. Conclusion

Figs. 4 and 5 depict the PSP simulation results of the circulator. TX-ANT/ANT-RX transmission losses of 3.3dB/4.5dB across a 100MHz BW centered at 1GHz. The simulated TX-RX isolation is higher than 25dB across this same bandwidth. Simulations indicate an overall power consumption of 48mW at the frequency of operation. Including a clock-boosting mechanism helps reduce the power consumed compared to conventional circuitry, which uses a chain of cascaded inverters.

V. Acknowledgment and Future Plans

I am grateful to have been chosen as a recipient of the IEEE MTT-S Undergraduate/Pre-Graduate scholarship, which has greatly assisted my efforts throughout the entirety of this project. Since receiving this honor, I have started my Ph.D. in Electrical Engineering at Columbia University in the City of New York. My motivation to pursue research in the field of integrated circuits has only been amplified since being chosen for this scholarship, and I wish to work on advancing the field of cryogenic electronics/quantum computing during the tenure of my doctoral studies and beyond.

References

[1] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A Millimeter-Wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3276–3292, 2017.

[2] A. Nagulu and H. Krishnaswamy, "Non-Magnetic CMOS Switched-Transmission-Line Circulators With High Power Handling and Antenna Balancing: Theory and Implementation," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1288–1303, 2019.

[3] A. Nagulu, T. Chen, G. Zussman, and H. Krishnaswamy, "Multi-Watt, 1-GHz CMOS Circulator Based on Switched-Capacitor Clock Boosting," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3308–3321, 2020.