Miniaturized Batteryless and Wireless Implants and Wearables for Stimulation and Sensing

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***Abstract*—This project brief presents a 12µW digitally configurable fully differential neural amplifier for neural sensing with an adjustable gain (38dB – 56dB) and bandwidth (0.5Hz to 10Hz – 10kHz) with no off-chip components. The total harmonic distortion is measured to be less than 0.2% at 4mVpp sinusoid at 1kHz (50dB gain) and a total input referred noise of 4µVrms in the 1Hz-10kHz bandwidth. The amplifier has a NEF of 5 with CMRR and PSRR > 60dB. The design is implemented in the standard 180nm technology. The amplifier is designed to be ultra-low power to be compatible with the batteryless and wireless implants that work on low harvested power in a fully wireless power transfer setup.**

***Index Terms*— Neural Signal Sensing, Local Field Potential (LFP), Action Potential (AP), Electrocardiogram (ECG), Bio-potential Sensing.**

I. INTRODUCTION

BATTERY-powered systems face challenges due to their bulky nature, the requirement for frequent charging in clinical studies, and the potential leakage of toxic chemicals. Patients universally prefer miniaturized implants and solutions that eliminate the need for charging or replacement. And, in some cases, replacement surgeries are not a feasible medical option. Consequently, wireless power transfer (WPT) technology is extensively employed to facilitate clinical experiments in a more convenient manner than their tethered counterparts and eliminates the need for battery power.

The predominant WPT technique is nearfield inductive coupling within the 3–40 MHz bands. While ultrahigh-frequency bands (300–3000 MHz) offer mid-field coupling, they encounter issues such as higher tissue attenuation and polarization misalignment. Therefore, most medical applications prefer WPT in the lower frequencies. However, lower frequencies necessitate larger dimensions for inductive loops to maintain high power transfer efficiency over large operating distances. This negatively impacts the implant size, which is undesirable. Hence, implants developed must be able to operate reliably at low harvested powers.

This scenario presents a new challenge, where we focus on the codesign of miniaturized inductive loops for implantable devices and ultra-low power circuits to make optimal use of the limited harvested power. To this extent, we develop ultra-low-power circuits to perform bio-potential sensing reliably with extremely low harvested powers.

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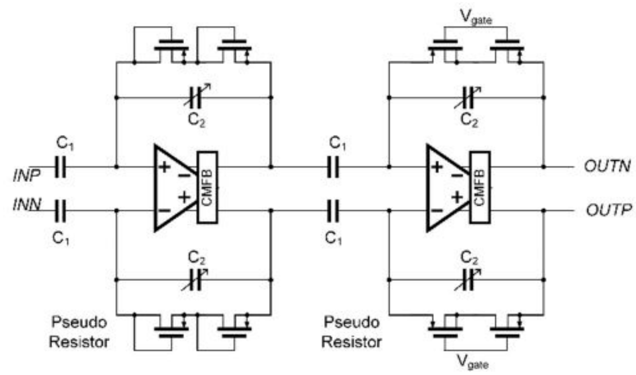

Fig. 1. Conceptual diagram of the neural amplifier.

The real-time sensing and transmission of neural signals have made significant strides in the treatment and understanding of neurological disorders. Action Potential (AP) signals, with a bandwidth of up to 10kHz, offer high spatial resolution down to the level of single neurons but are prone to instability and deterioration. In contrast, Local Field Potentials (LFP) signals, with a narrower bandwidth (up to 500Hz), provide stable but lower-resolution data, offering valuable insights into the brain's network-level dynamics. Both LFP and AP signals are typically recorded from the same electrode implanted in the brain.

II. NEURAL AMPLIFIER

The neural amplifier is designed as a capacitively coupled OTA as shown in Fig. 1 [1]. The gain of each stage in the capacitively coupled OTA is set by the ratio of the coupling capacitance (C1) to the feedback capacitance (C2). To ensure a high gain and low area requirement, a 2-stage amplifier is adopted over an equivalent single-stage amplifier as shown in Fig. 1. This is of prime importance as it is necessary to have a lower area per channel in the case of multi-channel sensing. All components are fabricated on-chip and no external components are used in the working of the neural amplifier chain enabling easy integration and scaling to multi-channel approaches. The high-pass corner frequency is set by the combination of on-chip pseudo resistors made from thick oxide transistors and feedback capacitors. The gain is adjusted by varying the capacitances in the feedback with a digitally controlled switch. The programmable codes allow for gain to be decreased in divisions of the power of 2 (1, 0.5, 0.25, 0.125). The high-pass corner frequency is controlled in the second stage with a gate-voltage tunable pseudo-resistor which can be tuned to allow for the lower cut-off corner to be modified from 0.5Hz to 10Hz.

The single-stage amplifiers are designed for broadband biopotential signals with a 3dB bandwidth of 10kHz. The input pairs for both stages are made using PMOS differential pairs to reduce the flicker noise contribution to the circuit which is prevalent at low frequencies in our bandwidth of interest [2]. The first stage is a folded cascode stage to allow for high gain and the second stage is a mirror OTA stage to allow for higher swings at the output. The overall characteristics of the neural amplifier are plotted in Fig. 2 with the different gain-bandwidth programming.

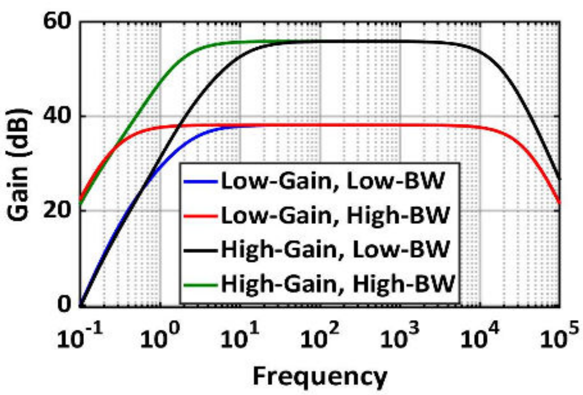

Fig. 2. Gain-Bandwidth with different digital code settings.

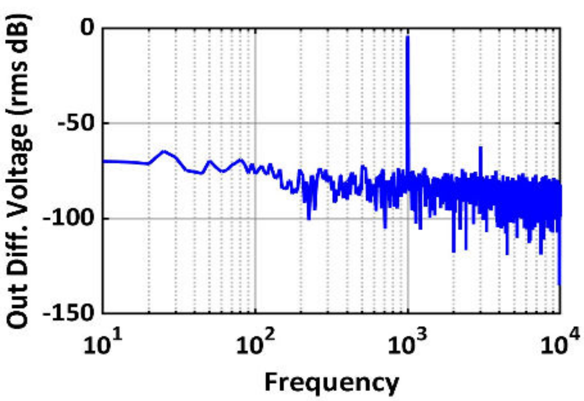

Fig. 3. THD less than 0.2% for a 4mVpp 1kHz sine input.

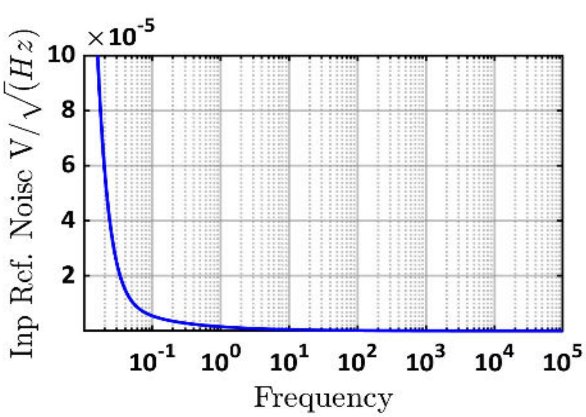

Fig. 4. Input referred noise. Integrated noise in 1Hz-10kHz BW is 4µVrms.

The measured THD is less than 0.2% at 4mVpp input sinusoid at 1kHz (50dB gain) as shown in Fig. 3. The input referred noise spectrum is plotted in Fig. 4 with the integrated noise in the 1Hz-10kHz bandwidth being 4µVrms. Table I gives an overview of the system metrics.

III. Conclusion

This brief presents an ultra-low-power neural amplifier with about 12µW power consumption designed to work for wireless and implantable applications in challenging WPT conditions with very low harvested powers. The neural amplifiers are digitally configurable fully differential amplifiers with an adjustable gain (38dB – 56dB) and bandwidth (0.5Hz to 10Hz – 10kHz) with no off-chip components. The total harmonic distortion is measured to be less than 0.2% at 4mVpp sinusoid at 1kHz (50dB gain) and a total input referred noise of 4µVrms in the 1Hz-10kHz bandwidth. The amplifier has a NEF of 5 with CMRR and PSRR > 60dB.

Acknowledgment And Career Plans

The IEEE MTT-S Scholarship program played a pivotal role in my graduate school by granting me the opportunity to participate in a tape-out, significantly contributing to my practical experience. It also enhanced my comprehension of low-power IC design, fostering a deeper understanding of these fields. Moreover, the scholarship heightened my research interest. Currently, I am pursuing my research under the guidance of Prof. Aydin Babakhani at UCLA. The foundation laid by the IEEE MTT-S Scholarship has been crucial in shaping my academic and research journey in these advanced areas of electrical engineering.

References

[1] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," in IEEE Journal of Solid-State Circuits, vol. 38, no. 6, pp. 958-965, June 2003, doi: 10.1109/JSSC.2003.811979.

[2] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw Hill, New York, 2017.

Table I. Overview of system specifications

Specification	Value
Target applications	Neural – (LFP, AP) & Cardiac – (ECG)
Technology	180nm
Supply voltage	1.2V
Off-chip components	Nil
Power	12µW (including bias, CMFB)
Gain	38dB-56dB (programmable)
Bandwidth (low corner)	0.5Hz-10Hz (programmable)
Bandwidth (high corner)	10kHz
THD	0.2% @ 4mVpp, 1kHz, (50dB gain)
Input referred noise	4µVrms (1Hz-10kHz)
NEF	5 (including bias gen, CMFB)
CMRR	>60dB
PSRR	>60dB