Wideband Frequency Synthesizer with Low Phase Noise in CMOS Technology for Multi-Band Wireless Application

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***Abstract*—In this report, we discuss the motivation, main idea, implementation, and measured results of our project that is focused on wideband frequency synthesizer with low phase noise in CMOS technology for multi-band wireless application. Firstly, a 21.8 to 41.6 GHz fractional-N sub-sampling PLL with dividerless unequal-REF-delay frequency-locked loop is introduced to achieve the low phase noise and low power consumption, simultaneously. Fabricated in a 40-nm CMOS technology, the PLL exhibits a fractional jitter from 133.3 to 159.2 fs. Consuming only 680μW, the URD-FLL ensures that the PLL is correctly locked to the target frequency. Secondly, a 0.2 to 39.2 GHz PLL using DAC-based constant control voltage compensator and quad-mode 2$^{\text{nd}}$ harmonic filtering oscillator is proposed, which obtains low phase noise and low spur over the wide output frequency range. Prototyped in a 40-nm CMOS technology, the PLL achieves 66.2 fs jitter and –71.3 dBc reference spur.**

***Index Terms*—CMOS, frequency synthesizer, frequency-locked loop, phase noise, sub-sampling, wideband.**

I. Introduction

To support multi-standard applications for wireless communications, the design of phase-locked loop (PLL) on a single chip is required to achieve the wide output frequency range, low phase noise, low spur, and low power consumption, simultaneously [1-2]. As a key component of PLL, the millimeter-wave (mmW) frequency dividers suffer from limited frequency range and consume the high power consumption. Therefore, mmW wideband PLL without divider should be investigated. Moreover, for a wideband PLL, large variation of VCO control voltage (V_C) exists in wideband frequency range. Due to the limited linear range of VCO and current matching range of charge pump (CP), such variation of V_C leads to large jitter and spur variations. Therefore, low variation of V_C is necessary for wideband PLL to achieve low jitter and low spur, simultaneously.

To address above issues, we proposed and developed a 21.8 to 41.6 GHz fractional-N sub-sampling PLL (SSPLL) with dividerless unequal-REF-delay frequency-locked loop (URD-FLL) [3] and a 0.2 to 39.2 GHz PLL using digital-to-analog converter (DAC)-based constant V_C compensator and quad-mode 2$^{\text{nd}}$ harmonic filtering oscillator [4]. Fabricated in 40-nm CMOS technology, the 21.8 to 41.6 GHz fractional-N SSPLL achieves the low phase noise and low power consumption. Meanwhile, the 0.2 to 39.2 GHz PLL shows the merits of low phase noise and low reference spur.

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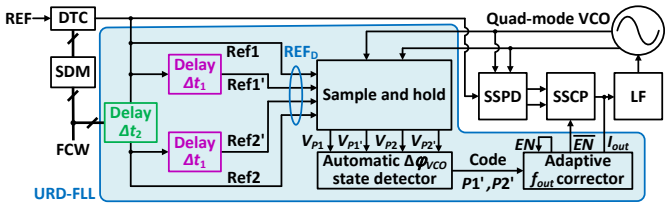

Fig. 1. Architecture of the proposed fractional-N sub-sampling PLL with URD-FLL.

II. Project Outcome

A. Fractional-N Sub-Sampling PLL with URD-FLL

Fig. 1 shows the block diagram of proposed fractional-N SSPLL with URD-FLL. Such URD-FLL consists of an unequal-delay references (i.e., REF$_D$) generator with the corresponding sample and hold circuits, an automatic VCO phase error ($\Delta\phi_{VCO}$) state detector, and an adaptive f_{out} corrector. The REF$_D$ generator includes two types of REF delay cells that generate Ref1, Ref1′, Ref2, and Ref2′. The slight delay Δt_1 is the time delay between Ref1′ and Ref1 or between Ref2′ and Ref2. The delay Δt_2 between Ref1 (Ref1′) and Ref2 (Ref2′) is equal to the target period of VCO signal. By controlling Δt_2, the proposed SSPLL is locked to desired frequency f_0. The REF$_D$ sub-samples the differential VCO signals and obtain four sampling points (i.e., $P1$, $P1'$, $P2$, and $P2'$). The sampling voltages V_{P1}, $V_{P1'}$, V_{P2}, and $V_{P2'}$ are used for the automatic $\Delta\phi_{VCO}$ state detector. By using the four sampling voltages, the quadrants of $P1$ and $P2$ in one period of the VCO are obtained. The quadrants of $P1$ and $P2$ represent the relationship between the periods of VCO output T_{VCO} and the target output period (i.e., defined by Δt_2). By comparing the quadrants of $P1$ and $P2$, the adaptive f_{out} corrector determines whether the output frequency has been locked correctly to f_0 or not. The EN is used to enable/disable the URD-FLL and I_{out} is utilized to correct the frequency. When f_{out}=f_0, EN=0 and I_{out}=0. Thus, the FLL doesn't affect the main loop phase locking and jitter performance. While the detected f_{out} doesn't equal f_0, EN is set to 1 and the f_{out} corrector generates the I_{out} to charge or discharge the loop filter, until f_{out}=f_0. Thus, the output frequency is locked to a specific frequency (i.e., 1/Δt_2), which achieves wideband correct frequency locking. The digital-to-time converter with sigma-delta modulator is introduced for fractional-N operation. A quad-mode oscillator is used to support the wide frequency range in mmW.

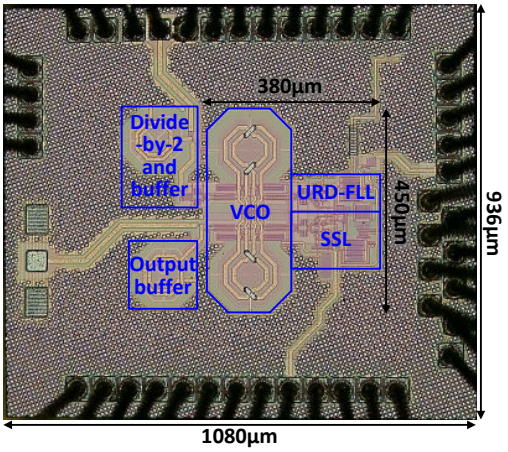

Fig. 2. Chip micrograph of the fractional-N sub-sampling PLL with URD-FLL.

The proposed fractional-N SSPLL is fabricated in a 40-nm CMOS technology. The chip micrography is shown in Fig. 2. The core size is 450μm×380μm. The proposed SSPLL achieves a 62.5% output frequency range from 21.8 to 41.6 GHz. The power consumption is from 11.6 to 14.8 mW, while the URD-FLL consumes 680 μW. The measured output fractional-N jitter is from 133.3 to 159.2 fs within the operation frequency range.

B. PLL with Constant Control Voltage Compensator

Fig. 3 shows the architecture of the proposed 0.2 to 39.2 GHz PLL. Such PLL consists of the mmW SSPLL, programmable divider chain, and multiplexer. A DAC-based constant V_C compensator is introduced in the SSPLL to achieve low jitter and low spur over wideband mmW frequency range. The V_C is preset as an optimal value $V_{C,opt}$ for minimized mismatch of CP current and variation of K_{VCO}. For the optimal DAC code preparation, the initial V_C (i.e., $V_{C,0}$) is compensated by ΔV_C to obtain a constant $V_{C,opt}$, while the $V_{C,opt}$ is given off-chip and ΔV_C is controlled by programmable code D_1. By comparing the $V_{C,0}$ and $V_{C,opt}$, the output of comparator (i.e., D_N) is used for DAC code calibrator. Once the calibration code D_C is unchanged, the preparation of optimal DAC code is finished. The code D_1 is stored as the optimal DAC code D_{opt}. Besides, a quad-mode 2$^{\text{nd}}$ harmonic filtering VCO is used to achieve low phase noise and over octave frequency range from 19 to 39.2 GHz. The tail resonator is injected in four times of common-mode current, which enhances the 2$^{\text{nd}}$ harmonic shaping. Then, the programmable divider chains and multiplexer are used to extend frequency range to 0.2-39.2 GHz. The frequency divider chains consist of current-mode logic (CML) dividers and true-single-phase-clock (TSPC) dividers. The CML dividers achieves wideband high frequency dividing and fully-quadrature outputs, while the TSPC dividers is used for low power consumption.

The proposed PLL is fabricated in a conventional 40-nm CMOS technology and occupies a 0.4 mm^2 core chip area. The chip micrograph is shown in Fig. 4. The whole PLL consumes

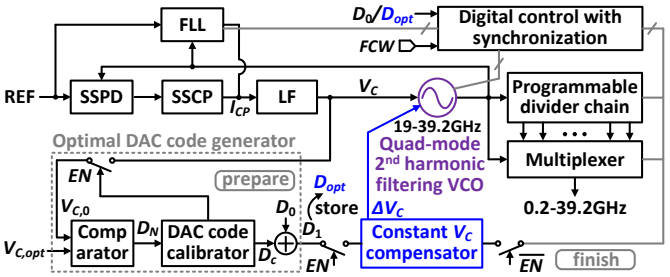

Fig. 3. Architecture of the proposed fractional-N sub-sampling PLL.

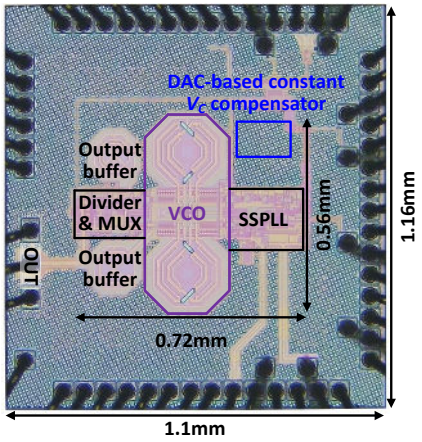

Fig. 4. Chip micrograph of the wideband PLL with constant VC compensator.

maximal 21.5 mW at 19–39.2 GHz with maximal 30.8 mW at 0.2–19 GHz. The reference frequency is 200 MHz. The measured output integrated jitters are 66.2 fs, 74.9 fs, 70.8 fs, and 87.7 fs, while the SSPLL locks to 19 GHz, 24 GHz, 28 GHz, and 34 GHz, respectively. The reference spur is –71.33 dBc with DAC ON.

III. Fellowship Impact and Career Plan

It is a great honor for me to receive the 2023 IEEE Microwave Theory and Technique Society Graduate Fellowship Award, which supports my research work and obtains a valuable research experience. I plan to continue my research after graduation to further develop the high performance frequency synthesizer in industry. Finally, I would like to thank my supervisor Prof. dr. Xun Luo for the guidance and encouragement during my research.

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