An Efficient 0.4 THz Radiator with 20.6 dBm EIRP and 0.2% DC-to-THz Efficiency in 90nm SiGe BiCMOS

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***Abstract*— This paper presents an efficient 0.4 THz single-element radiator implemented in 90nm SiGe BiCMOS. It consists of a PIN diode quadrupler, where a mm-wave Colpitts oscillator at 100 GHz drives a PIN diode switching-reactance-multiplier into reverse recovery. This idea is an extension on the idea of using PIN for pulse generation, which was submitted initially to MTT application. In this idea, the PIN diode abruptly switches between two impedance states and produces strong harmonics. Harmonic injection locking is also presented in this work, where two quadrupler cells are mutually interlocked, and their fourth harmonic power at 0.4 THz combines at the antenna. The radiator achieves a peak EIRP of +20.6 dBm and -5.8 dBm radiated power at 398 GHz, with a 10.7 % tuning range, and consumes 130 mW DC power.**

***Keywords*— PIN diode, multiplier, THz source, SiGe**

I. Introduction

The THz band (0.1-10 THz) has several unique properties, making it a potential candidate for imaging, spectroscopy, and communication applications. These applications require efficient high-power THz generation over a wide frequency range. Due to the limited f_T/f_{max} of transistors, direct THz generation is not feasible, and harmonic generation using non-linear devices such as transistors or varactor diodes is popularly used [1-4]. However, these devices have weak non-linearity, limiting the amount of generated THz power. PIN diodes have shown strong non-linearity and have been used for THz generation [5], [6].

This work presents an efficient 0.4 THz single-element radiator based on PIN diode switching reactance frequency multipliers (SRM). Due to reverse recovery, PIN diodes are strongly non-linear and are hence used here to maximize DC-to-THz generation efficiency. To improve the power, on-chip power combining at the antenna node is adopted, where two quadruplers are mutually interlocked, and the 0.4 THz signal adds in-phase. Performing power combining at the antenna ensures low loss, and the THz signal is directly radiated.

II. PIN Diode and Reverse Recovery

The reverse recovery of PIN diodes is used in this idea for efficient THz generation. A PIN diode consists of p+ and n+ regions, separated by an intrinsic ‘I’ region. The presence of the ‘I’ region differentiates a PIN diode from conventional diodes. A standard PIN diode from GlobalFoundries 90nm process is used here and is illustrated in Fig. 1 (a). Fig. 1 (b), (c) demonstrate the operation of a PIN diode when a large-signal sinusoidal voltage is applied across it. In the

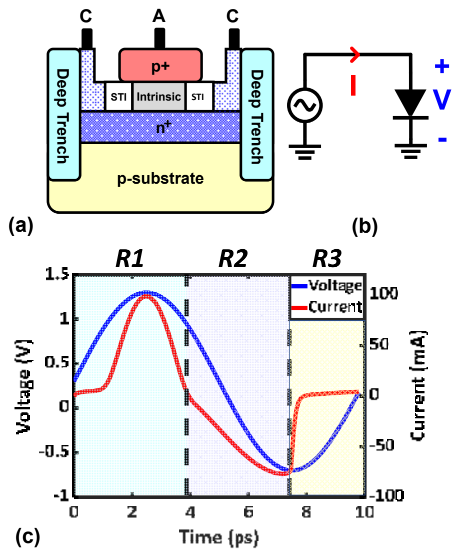

Fig. 1. (a) PIN diode illustration (b) PIN diode excited by a voltage source (c) Current through the PIN diode when excited by a 100 GHz voltage source

forward mode of operation (R1), the diode conducts, and the I-region is filled with electrons and holes to facilitate forward conduction. Because of these excess carriers, the diode remains ON and continues current conduction in the reverse mode (R2) until all excess carriers are depleted. This is different from a conventional diode, where there is no carrier storage, and the diode stops conducting as soon as it leaves R1. Once the carriers in the PIN diode are depleted, the current snaps to zero (R3), exhibiting reverse recovery. This switching is abrupt, and the generated waveform is rich in harmonics. During a typical drive cycle, the diode operates across the conduction regions (R1 and R2) and the OFF state region (R3). In R1 and R2, ideally, the diode can store any amount of charge at a constant voltage (turn-on voltage of the diode). In R3, the diode behaves like a small capacitance.

III. Circuit Design

The PIN diode quadrupler design is explained in this section. It consists of a mm-wave oscillator at 100 GHz that drives a PIN diode. Two quadruplers are interlocked, and the power at 0.4 THz is combined and radiated through an on-chip antenna.

A. Switching Reactace Multiplier

PIN diode multipliers are Switched Reactance Multipliers (SRMs), where the diode switches abruptly from a short to

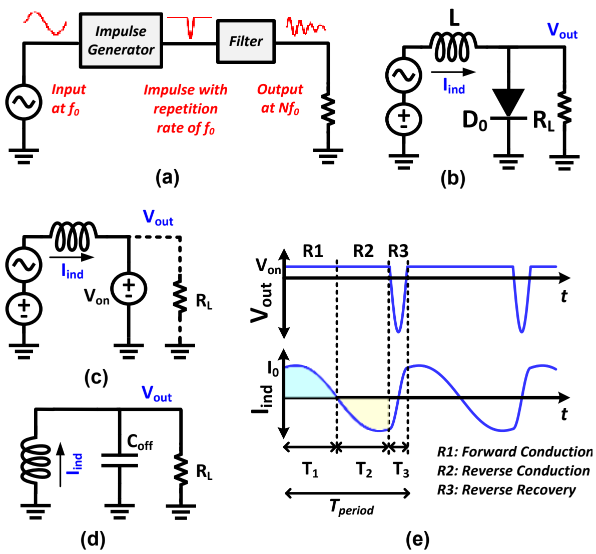

Fig. 2. (a) A switched reactance frequency multiplier (b) PIN diode impulse generator (c) Equivalent circuit during R1 and R2. (d) Equivalent circuit during R3. (e) V_{out} and inductor current

a high impedance state. The fast switching behavior enables efficient THz generation using PIN didoes. This differs from conventional varactor or transistor-based multipliers where the reactance variation, although non-linear, is gradual (Variable Reactance Multiplier, VRM). SRMs were designed in the past using discrete microwave step-recovery diodes (SRD) [7]. However, they are not available in modern silicon processes. This work extends the SRM theory to PIN diodes since they behave similarly to SRDs under large-signal operation.

Fig. 2 (a) illustrates a general SRM circuit. It consists of an impulse generator circuit that is excited at a frequency f_0. This generates an impulse that can be filtered to extract the harmonic of interest at 'Nf_0'. The impulse train generator circuit is shown in Fig. 2 (b). A PIN diode is connected to an RF source through an inductor and to a load R_L. The non-linear time-varying behavior of the PIN diode can be analyzed by replacing the diode with the linear switching model and applying boundary conditions. The simplified circuit is shown in Fig. 2 (c), (d). This circuit is solved using linear analysis, and the resulting diode voltage (V_{out}) and inductor current (I_{ind}) are plotted in Fig. 2 (e). Regions R1, R2, and R3 correspond to forward conduction, reverse conduction, and reverse recovery mode. During forward and reverse conduction (R1, R2), the PIN diode is ON and clamped to the diode turn-on voltage V_{ON}. Charges stored in the 'I' region of the diode during R1 are depleted during R2, and the diode turns OFF at R3 when this charge becomes zero (Q1 = Q2). We bias the diode such that it carries peak reverse current at the onset of R3. Even though the diode turns OFF, current continuity through the inductor must be maintained. This results in a sharp negative impulse voltage at V_{out}. The height and width of this impulse depend on C_{OFF} and R_L. This impulse is then filtered to extract the harmonic of interest at Nf_0.

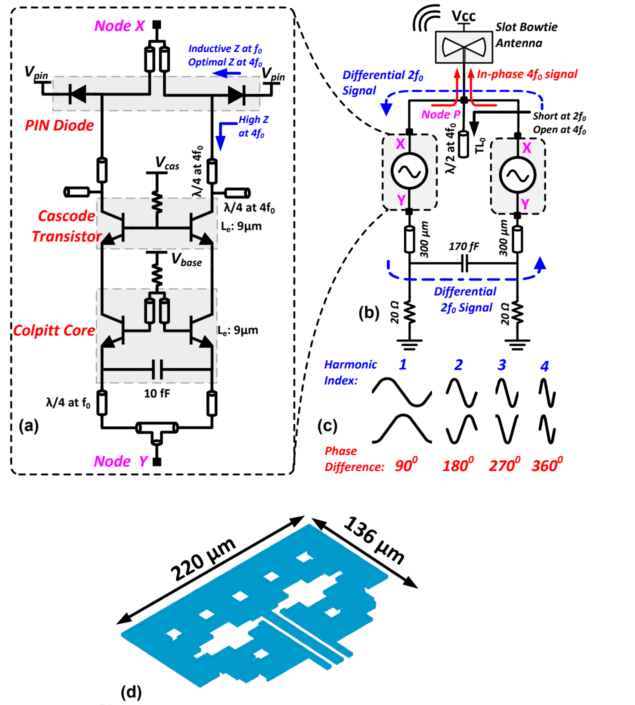

Fig. 3. (a) PIN diode switched reactance multiplier at 100 GHz (b) Quadrature locking and power combining (c) Odd mode coupling at 2nd harmonic provides quadrature and in-phase signals at 1st and 4th harmonics respectively (d) Slot bowtie antenna

B. THz Transmitter Design

Fig. 3 (a) shows the schematic of the PIN diode-based THz SRM quadrupler. It consists of a differential mm-wave Colpitts oscillator, which oscillates at 100 GHz. A cascode stage is used to amplify the oscillator output and isolate the oscillator core. Transmission line (TL) matching networks connect the cascode to the diode and extract the 4th harmonic at 400 GHz. These matching networks ensure that (1) the 100 GHz signal is large-signal matched to the diode and (2) the antenna is matched to the diode at the 4th harmonic at 400 GHz. The amount of generated THz power depends on the diode size. Choosing a diode size that has high (C_{ON}/C_{OFF}) ensures the diode switches between widely different impedance levels. Choosing a diode size with low R_S ensures high Q. Thus, the diode size, which maximizes the ratio (C_{ON}/C_{OFF})/R_S, is chosen and this consequently maximizes the generated THz power.

On-chip power combining at the antenna is used in this work. Two quadrupler cells are mutually locked at 100 GHz to boost the power at 400 GHz. Fig. 3 (b) shows the locking mechanism. Node X of both the quadrupler cells are directly connected to the antenna and to an open line TL_0, which is $\lambda/2$ length at 400 GHz. Only even harmonics of the quadrupler cells can interact with each other at node X since it lies on the common mode of the individual cells. The oscillators undergo mutual injection locking and can operate in the odd mode or even mode of the second harmonic. However, TL_0 creates a

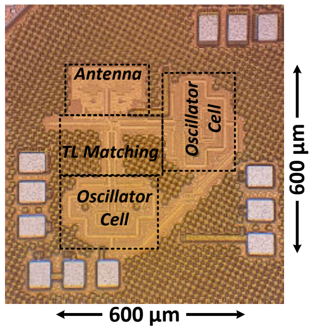

Fig. 4. Die Micrograph

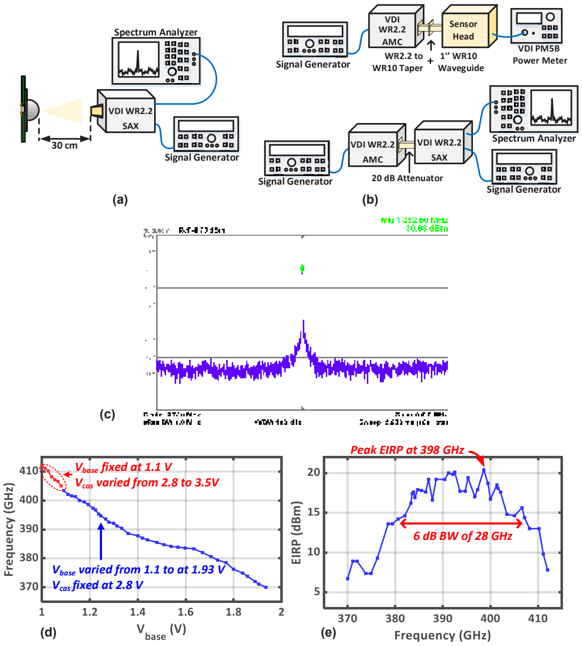

Fig. 5. (a) EIRP measurement setup (b) VDI WR2.2 SAX loss calibration (c) Measured spectrum at 398 GHz (d) Frequency tuning curve (e) EIRP variation vs frequency

short at node P at the second harmonic. This prevents the even mode signals from coupling. For odd mode, node P is a virtual ground and remains unaffected by TL_0. Thus odd mode oscillation is sustained at the second harmonic. Consequently, due to harmonic injection locking, the oscillators become quadrature locked at the fundamental frequency and in-phase locked at the 4th harmonic (Fig. 3 (c)). At node Y, since the oscillators cannot be directly connected due to layout constraints, they are connected through 300 μm TLs and coupling capacitors. Resistors are used for biasing.

A slot-bowtie antenna is used in this work. Fig. 3 (d) shows the structure of the antenna. Additional slots are added to the antenna to meet density requirements. The antenna is used with a hyper hemispherical silicon lens. Since only one antenna is used, it can be aligned to the axis of the lens.

IV. Measurement Results

The design is fabricated in GlobalFoundries 90nm SiGe BiCMOS process. It consumes 130 mW DC power in nominal operation. Fig. 4 shows the die micrograph. The design occupies an active area of 0.36 mm^2.

The chip is wire-bonded to a PCB, and a hyper hemispherical silicon lens is attached. The lens helps improve radiation efficiency by removing substrate modes, and increases the directivity. No substrate thinning is employed. Fig. 5 (a) shows the free space measurement setup. The chip is kept at a 30 cm far-field distance from a VDI WR2.2 mixer (SAX). The conversion loss of the mixer is measured using a VDI WR2.2 signal generator extender (AMC), which is calibrated using a VDI PM5B power meter using the setup shown in Fig. 5 (b). The measured spectrum at 398 GHz is shown in Fig. 5 (c). An EIRP of 20.6 dBm is obtained after de-embedding the losses. The frequency is varied by changing the base and cascode bias. This is plotted in Fig. 5 (d). A tuning range of 42 GHz (10.7 %) is measured. The EIRP variation across frequency is plotted in Fig. 5 (e), and a 6 dB bandwidth of 28 GHz is measured.

V. Career Plan Acknowledgment

I should thank MTT-S community for selecting me for IEEE MTT-S Graduate fellowship. This prestigious award is an great honor for me, and further motivates me to contribute in this research domain. I would like to thank my advisor Prof. Aydin Babakhani and my colleague Sidharth Thomas for their help and support. Moreover, I am going to start my career in industry to learn more about this field in a different environment than academia. Hopefully, with my experience in academia and the knowledge I gain in industry, I can contribute more to the field of microwave and circuit design and keep on innovating.

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