Wideband High Data-Rate Digital Transmitter Array with Enhanced Peak/Average Efficiency in CMOS Technology for Wireless Applications

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***Abstract*—In this report, the motivation, idea, and results of wideband digital transmitter (TX) array with power back-off (PBO) efficiency enhancement in CMOS Technology. Firstly, the quadrature switched/floated capacitor power amplifier (SFCPA) is introduced to improve power back-off efficiency. The SFCPA is introduced to decrease the dynamic power consumption at PBO, which could improve the system efficiency. Implemented in 40-nm CMOS, the proposed DPA with 1.2/2.4V supply achieves 30.3 dBm saturated output power (P_{out}) with 36.6/32.9/29.1/23.7/18.6/13.2% system efficiency (SE) for 0/3/6/9/12/15dB PBOs at 2.4GHz. Secondly, a 4-element digital-modulated phased-array TX based on SFCPAs and reconfigurable switched-capacitor tuning lines (RSCTLs) is proposed. The fabricated phased-array TX features 28.4dBm peak output power and 37.9% peak SE. It supports 0/3/6/9/12/15-dB PBOs efficiency enhancement and 15-bit phase-tuning resolution.**

***Index Terms*—CMOS, Doherty, IQ cell sharing, power amplifier, reconfigurable self-coupling canceling transformer (RSCCT), switched/floated capacitor power amplifier (SFCPA).**

I. Introduction

THE future wireless communication transmitter (TX) systems demand the wideband operation to support multi-standards. Meanwhile, the increasing requirement on high speed access also requires power amplifiers with high linearity and large dynamic range to support high-order modulation signals. In addition, the lower power consumption is required, especially for portable devices. CMOS digital power amplifiers (DPAs) exhibit merits of high peak efficiency and low cost [1], [2]. However, the modulation signal with large peak-to-average-power ratios (PAPRs) in wireless communication leads to efficiency degradation of conventional DPAs. Thus, high efficiency, especially at power back-off (PBO) for enhanced average efficiency is demanded in PAs. Besides, phased-array TXs with beam-steering are dramatically demanded in future wireless communication systems, which need high resolution and low gain/phase error.

In this report, we proposed and developed a quadrature switched/floated capacitor power amplifier (SFCPA) [3], and a phased-array TX based on quadrature SFCPA [4]. Fabricated in 40-nm CMOS technology, the quadrature SFCPA achieves high peak and average efficiency, watt-level output power, low cost, and high integration level. The phased-array TX shows the merits of high phase-tuning resolution and significant efficiency enhancement.

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II. Project Outcome

The block diagram of the proposed quadrature SFCPA is shown in Fig. 1(a). The SFCPA is introduced to decrease the dynamic power consumption, which benefits for PBO efficiency enhancement. Meanwhile, the technique of hybrid Doherty and impedance boosting utilizes the reconfigurable matching network with controllable impedance turn ratio to boost load impedance of PA at PBO, which further improves PBO efficiency [5]. The Main and Aux. PAs are composed of 4 identical differential IQ cell shared sub-PA arrays. Each sub-PA consists of 6-bit MSB and 1-bit LSB unit cells. The unit cells can be switched among three operation states (i.e., ON, OFF, and FLOAT). The output matching is composed of the 4-to-1 reconfigurable self-coupling transformer (RSCCT) with switched capacitor C_t and output capacitor C_{out}. The turn ratio of RSCCT can be controlled to achieve impedance boosting, which further improves the PA efficiency at PBO.

The schematic of the unit cell based on SFCPA is shown in Fig. 1(b). The cascode inverter structure with 2VDD supply is used in SFCPA unit cell to deliver higher output power. LOI and LOQ are quadrature LOs with 25% duty cycle. BBI and BBQ are BB control signals for in-phase and quad-phase, respectively. EN is the enable signal of "FLOAT" state. The detailed operation of the SFCPA unit cell is illustrated as shown in Fig. 1(b).

The proposed quadrature SFCPA with RSCCT is fabricated in 40nm CMOS technology, which occupies 2mm $\times$ 1.1mm including all I/O pads with 1.2/2.4V supply, as shown in Fig. 2. The proposed SFCPA features a peak P_{sat} of 30.3 dBm with DE of 41.3% and SE of 36.5% at 2.4 GHz. It achieves DE of 41.3%, 37.5%, 36.1%, 30.9%, 26.2%, 20.2% at 0, 3, 6, 9, 12, 15dB PBOs. The measured 60MHz 256-QAM signal, it features P_{avg} of 23.32dBm with average DE of 30.7%, EVM of –31.9dB, and ACLR$\leqslant$–30dBc. Besides, the 40MHz 1024-QAM signal is also supported by the proposed SFCPA, which exhibits P_{avg} of 20.44 dBm with average DE of 22.6%, EVM of –35.9dB, and ACLR$\leqslant$–34.88dBc.

Based on the quadrature SFCPA, the 4-element phased-array TX is proposed, as shown in Fig. 3. It consists of four digital quadrature TXs, a 1-by-4 power divider, and digital circuits including quadrature rotator, decoder, etc. 2$\times$2 array topology is utilized. The input LO signals are divided by the active power divider into four signals with identical amplitude and phase. The RSCTL is used to shift the LO signals with fine phase tuning. An active balun circuit and a differential

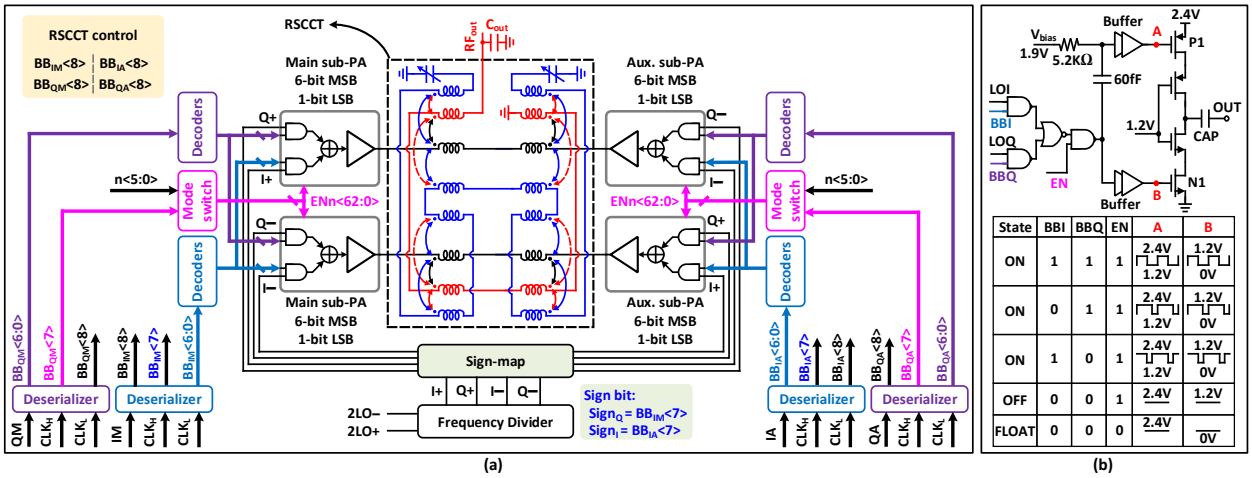

Fig. 1. (a) Block diagram of the proposed SFCPA. (b) The schematic and detailed operation of SFCPA unit cell.

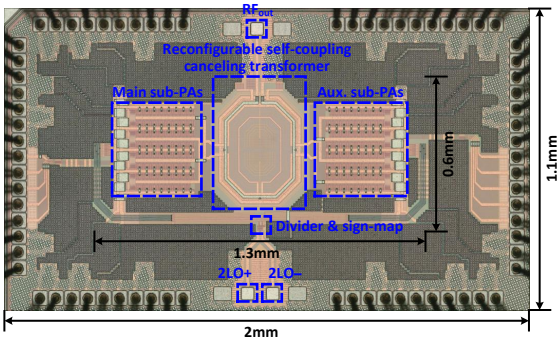

Fig. 2. Die micrograph of the quadrature SFCPA.

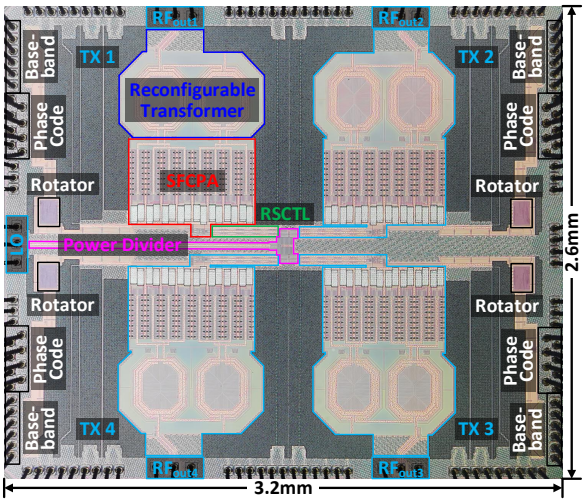

Fig. 3. Die micrograph of the 2×2 digital-modulated phased-array TX.

frequency divider (FD) convert the LO signals into quadrature carrier signals for the quadrature SFCPAs. Moreover, quadrant selection of the SFCPAs is achieved by a sign-map (SM) circuit. Unlike conventional digital quadrature TX, the proposed SFCPA can not only generate the modulated signals, but also perform coarse phase tuning. A 5-bit resolution is implemented in the SFCPAs with quadrature rotation. Besides, to further improve the resolution of phase tuning, the 10-bit reconfigurable switched-capacitor tuning lines (RSCTLs) is introduced.

The proposed 2×2 digital-modulated phased-array TX is fabricated in 40-nm CMOS technology. Each transmission channel delivers a saturated output power of 26.5–28.4dBm from 2 to 4GHz. Meanwhile, the system efficiency is 27.1%–37.9%. The measured RMS phase and power errors are 0.12°–0.51° and 0.15–0.24dB over 2–4GHz, respectively. The proposed TX supports 25MHz 256-QAM with P_{avg} of 21.5dBm, average system efficiency of 23.2%, EVM of –33.1dB, and ACLR $\leq$ –34.1dBc.

III. Fellowship Impact and Career Plan

It is a great honor for me to receive the 2021 IEEE MTT-S graduate fellowship Award, which supports my research work and will encourage me in the future academic career. I plan to continue my research to further develop the high data-rate high efficiency digital TX for wireless systems. Finally, I would like to thank my supervisor Professor Xun Luo, and Associate Professor Huizhen Jenny Qian, for the guidance and encouragement during my research.

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