1.2–2.8 GHz 32.4 dBm Digital Power Amplifier with Balance Compensated Matching Network

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***Abstract*—In this paper, a wideband watt-level digital power amplifier (DPA) with balance compensated matching network is proposed for polar transmitters. The balance response of the differential to single-ended transformer is enhanced by the series-loaded compensation capacitor, which leads to improved efficiency. To verify the mechanisms mentioned above, a prototype DPA is fabricated in a conventional 40-nm CMOS technology. The proposed DPA operates over 1.2–2.8 GHz and exhibits peak output power of 32.4 dBm at 2 GHz and a peak drain efficiency of 53.8% at 1.8 GHz. It supports up to 10MHz 1024-QAM with P_{avg} of 22.14 dBm, EVM of –35.75 dB, ACPR of –35.37 dBc.**

***Index Terms*—Balance compensated matching network, digital power amplifier (DPA), efficiency enhancement, watt-level, wideband.**

I. Introduction

With the development of wireless communication, power amplifiers (PAs) with high-power, energy efficient, low supply, and low cost are highly demanded. CMOS analog PAs with high power and linearity is highly developed. However, the system efficiency is relatively low due to extra modules. Digital PAs (DPAs) exhibit enhanced efficiency and medium output power. A watt-level CMOS DPAs with merits of wideband, high efficiency, low supply, and compact size still remain great challenges. In this letter, a 1.2–2.8 GHz watt-level DPA with balance compensated matching network is proposed. Such matching topology is consisted of a 4-to-1 transformer with a compensated series-loaded capacitor. A prototype DPA is implemented and fabricated using a conventional 40-nm CMOS technology, which exhibits 32.4 dBm peak output power and 53.8% peak drain efficiency (DE) under a 1.1/2.5V supply.

II. Circuit Design

The block diagram of the proposed wideband watt-level DPA based on a balance compensated matching network is shown in Fig. 1. A 4-way series combining architecture is adopted. Each switch array consists of 6-bit unary MSB cells and 4-bit binary LSB cells with cascode 2.5 V thick-oxide transistors, 2.5 V digital AND gates and buffers. Meanwhile, the matching network performs the 4-way power combining, differential to single conversion, wideband impedance matching, and balance compensation, simultaneously. Besides, two sets of parallel high speed 5:1 deserializer and encoder are used to convert the serial baseband signals to thermometer and binary codes.

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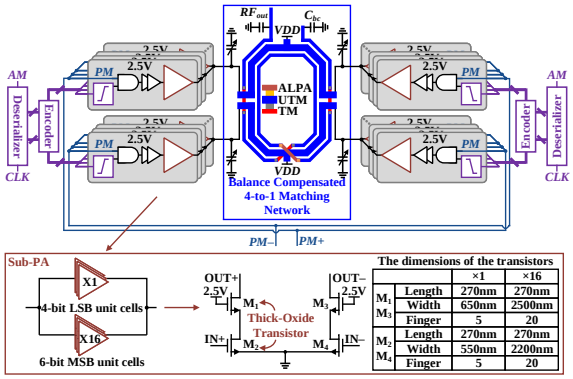

Fig. 1. Block diagram of the proposed watt-level digital power amplifier.

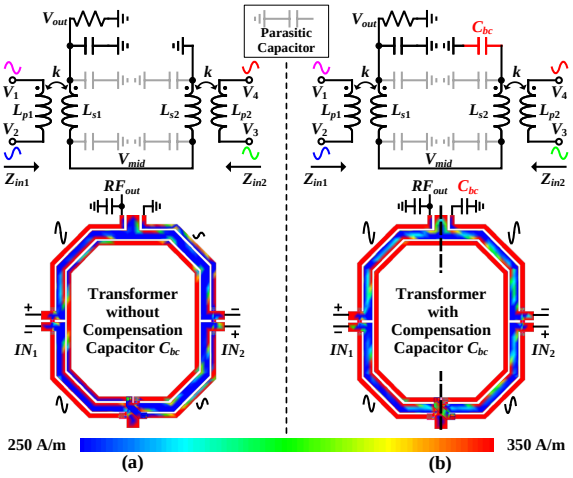

Fig. 2. Simplified circuit of the (a) conventional and (b) proposed. The current density of transformers (c) without and (d) with a compensated capacitor C_{bc}.

A. Matching Network with 4-to-1 Transformer

Higher output power can be achieved with increased drain current, i.e., smaller Z_{in} of the transformer once the voltage swing remains the same. Such operation leads to a larger inductance ratio of the transformer. However, such ratio is limited due to the Q degradation. In the proposed DPA, series power combining scheme is used. In this way, the inductance ratio is reduced and lower passive loss is achieved.

B. Imbalance Compensation Technique

The simplified circuits of 4-way power combiners are depicted in Fig. 2(a) and (b). A compensation capacitor C_{bc} marked in red is introduced, as shown in Fig. 2(b). Compared with transformer without compensation in Fig. 2(a), it is notable that Fig. 2(b) exhibits uniform current distribution for

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART HIGH-POWER POWER AMPLIFIERS

	This Work			JSSC2019 [1]		ISSCC2019 [2]	ISSCC2019 [3]	JSSC2012 [4]
CMOS Tech.	**40-nm**			28-nm		65-nm	40-nm	0.18-um with IPD technology
Architecture	**Digital Polar with Balance Compensated matching**			Digital Polar	Digital Quadrature	Phase-interleaved SCPA	Single-supply Class-G SCPA	Analog with Triple-mode
Resolution	**10-bit**			10-bit	9-bit	N/A	13-bit	N/A
Supply (V)	**1.1/2.5**			1.1/2.2		2.4/3.6	2.2	3.4
Frequency (GHz)	**1.2–2.8**			2–2.7		1.5–2.3	0.699–0.915	1.95
Peak Power (dBm)	**32.4**			28.8	26.3	30	27.1	28.4
Peak Efficiency	**53.8% DE 43.8% PAE**			30.8% PAE	22.9% PAE	45.9% DE	33.3% PAE	40.7% PAE
Modulation	**64-QAM 50 MHz**	**256-QAM 25 MHz**	**1024-QAM 10 MHz**	256-QAM 20 MHz	256-QAM 20 MHz	16-QAM OFDM	Cat-M1 16-QAM 1.4 MHz	3-GPP
Avg. Power	**25.37 dBm**	**24.13 dBm**	**22.14 dBm**	21.40 dBm	16.76 dBm	22.8 dBm	22.6 dBm	16.5 dBm
EVM	**–26.97 dB**	**–31.67 dB**	**–35.75 dB**	–30.7 dB	–30.2 dB	–24.7 dB	–30.2 dB	N/A
Area (mm^2)	**2.898**			0.5625*		7.2	5	2.12 + 0.66**

*: Core size; **: Whole circuit size + integrated passive device (IPD) size

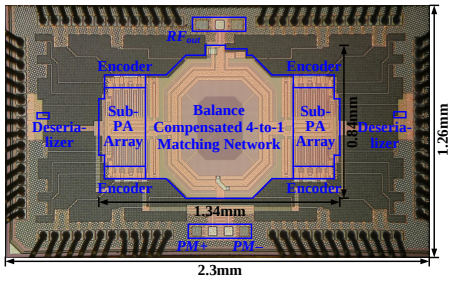

Fig. 3. The chip photograph of the proposed digital power amplifier.

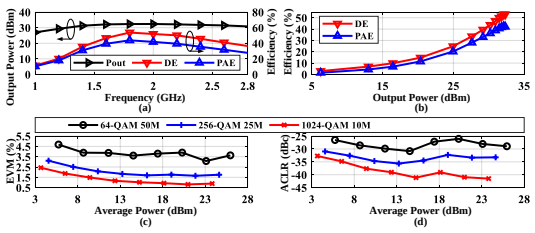

Fig. 4. Measured (a) output power, drain efficiency (DE), and power added efficiency (PAE), (b) DE and PAE versus output power, (c) EVM and (d) ACLR versus average output power.

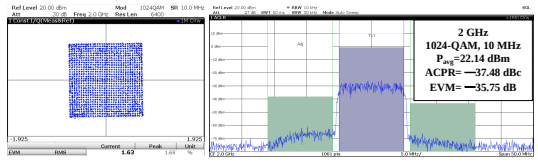

Fig. 5. Measured constellation diagram constellation diagrams and spectrum under different modulations at 2 GHz.

the entire secondary coil, which leads to enhanced impedance balance. And thus, the compensated transformer is capable of higher efficiency and power.

III. RESULT

The proposed watt-level wideband DPA fabricated using a conventional 40-nm CMOS technology. The photograph is in Fig. 3. The chip size and core size are 2.3 mm × 1.26 mm and 1.34 mm × 0.84 mm, respectively. The supply is 1.1/2.5V. The measured results of output power, DE, and power added efficiency (PAE) are depicted in Fig. 4. Meanwhile, the peak output power, DE, and PAE are 32.4 dBm, 53.8%, and 43.8%, respectively. As shown in Fig. 5, the 10 MHz 1024-QAM signal with EVM of –35.75 dB is achieved at 2 GHz, Table I shows the comparison with state-of-the-art high-power DPAs.

IV. CONCLUSION

In this letter, a wideband watt-level high efficiency DPA based on balance compensated matching network is proposed. To achieve high output power with a compact size, the 4-to-1 combining transformer is introduced. Meanwhile, to decrease the imbalance, the imbalance compensation capacitor is utilized. The proposed DPA fabricated in 40-nm CMOS technology shows the merits of watt-level output power, high efficiency, and wide bandwidth.

V. ACKNOWLEDGMENT AND NEXT PLAN

I would like to thank my supervisor Associate Professor Huizhen Jenny Qian for her guidance on radio-frequency integrated circuits (RFIC) design. I am also extremely grateful to IEEE and MTT-S for encouraging me to take up this research. With the support of the funding and my supervisor Associate Professor Huizhen Jenny Qian, I have published one MWCL paper [5]. I will continue to study in this field to become an excellent RFIC designer and make more progress in excellent and efficient communication for human being.

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