A Low-Loss Ultra-Compact Folded Inductor-Based Bandpass Filter for 5G NR Applications

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***Abstract*—An ultra-compact folded inductor-based mm-Wave bandpass filter for 5G NR applications is presented. The proof-of-concept design is realized in GlobalFoundries 45nm RF-SOI process with a core chip area of 128 µm × 128 µm and is characterized to validate the simulation results. The measurement results closely match the simulation results with a <3-dB insertion loss over 16 – 40 GHz, >10-dB return loss over 19 – 42 GHz, and a minimum insertion loss of 1.05 dB at 27 GHz. Overall, the proposed bandpass filter attains a fractional bandwidth of 71% (21 GHz bandwidth from 19 – 40 GHz) with a 1.19-dB insertion loss at the center frequency of 30 GHz, outperforming the state-of-the-art bandpass filter designs.**

***Index Terms*—5G NR, CMOS, mm-Wave, ultra-compact, bandpass filter, folded inductor-based, Ka-band.[1]**

I. Introduction

Millimeter-wave (mm-Wave) 5G NR communications prompted the development of mm-Wave phased array transceiver systems for high-speed and low-latency satellite communications, Internet of Things, and biomedical applications [1]. Passive components, such as bandpass filters, are fundamental building blocks for attenuating the interferences outside the desired frequency band of the mm-Wave frontend systems necessary for channel modulation and spectral planning. Conventional mm-Wave BPF designs often use coupled transmission lines (T-lines) and stubs [2–3]. However, T-lines and stubs significantly increase the BPF chip area, resulting in a bottleneck for compact mm-Wave frontend integration for scalable MIMO arrays. Furthermore, long T-lines are inherently lossy and narrowband, which degrades the filter's performance such as bandwidth, gain, and selectivity.

To overcome these issues, we propose a low-loss, ultra-compact, Ka-band BPF core within only one inductor footprint for a substantial area reduction and loss improvement. This design methodology has previously been implemented for other passive components [4], and, in this project, a third-order BPF is presented for its Ka-band implementation.

II. Folded Inductor-Based Bandpass Filter

A general BPF circuit is comprised of shunt and series inductors and capacitors, whose values are determined to minimize the insertion loss of the component at the center frequency and determine the location of the transmission poles and zeroes in the passband response. Each inductor-capacitor pair forms an element, which is connected to other elements to form a ladder-like circuit. Therefore, a lossless third-order BPF is modeled in a T-equivalent format as shown in Fig. 1, where C_n and L_n from n=1–3 are the capacitance and inductance values for nth section, respectively, and Z_0 is the characteristic impedance of the ports.

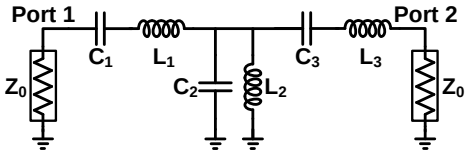

Fig. 1. T-equivalent lumped-element model of a third-order BPF.

This lumped-element third-order BPF model requires 3 on-chip inductors and capacitors. Implementing every inductor on a separate footprint would significantly increase the area. Hence, to minimize the area, all inductors and capacitors are implemented within one folded inductor footprint, requiring only another inductor to provide the desired response in the proposed BPF design.

III. Simulation and Measurement Results

The proof-of-concept design was fabricated using GlobalFoundries 45 nm RF-SOI CMOS process. For this design, a characteristic impedance, Z_0, of 50 Ω was chosen. A measurement setup was prepared with a GSGSG probe where Ports 1 and 2 were used as two single ports. Scattering parameter measurements were taken with Keysight 67 GHz 4-port vector network analyzer (N5247B) after SOLT calibration. The micrograph of the fabricated design is shown in Fig. 2.

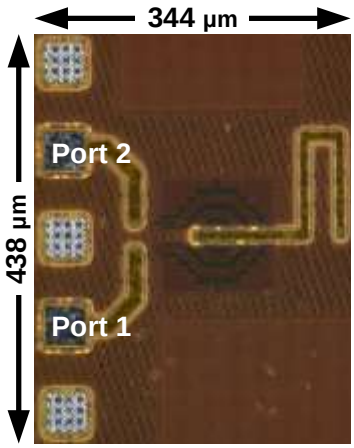

Fig. 2. Chip micrograph of the proposed folded inductor-based third-order BPF realized in GlobalFoundries 45 nm RF-SOI CMOS process.

Both simulation and measurement results between 10 – 50 GHz are shown in Fig. 3. All three resonance points corresponding to the resonances of the unit elements are

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Table 1. Performance comparison of CMOS mm-Wave BPFs

Reference	Technology	Topology	Center Freq (GHz)	Fractional Bandwidth (%)	Stopband Attenuation (dB)	Insertion Loss (dB)	Size (mm^2)	Normalized Size (λ^2) at f_c
[2]	130 nm SiGe Bi-CMOS	Broadside-coupled meander line	35.5	73	35	3.1	0.016	0.00022
[3]	130 nm SiGe Bi-CMOS	Broadside-coupled split-ring	40	20	20	1.7	0.012	0.00021
[5]	130 nm SiGe Bi-CMOS	Multi-layer ring	31	35	>45*	2.2	0.0244	0.00026
[6]	130 nm SiGe Bi-CMOS	Cross-shaped line	23.5	38	50	3.8	0.017	0.00010
This work	**45 nm RF-SOI CMOS**	**Folded inductor**	**30**	**71**	**20**	**1.19**	**0.0164 (0.0364 with L_2)**	**0.00016 (0.00035 with L_2)**

*Inferred from the S21 parameter response.

observed in the return loss measurements, confirming the successful demonstration of a third-order BPF. The discrepancy between the 3D EM simulation results and measurement results could be attributed to the parasitics, especially parasitic capacitances, introduced by the probes and the pads that shift the resonance frequencies of the S-parameter responses higher.

Performance comparison of this design with existing published on-chip BPF designs is shown in Table 1.

IV. Conclusion

A proof-of-concept mm-Wave Ka-band third-order BPF design realized in 45 nm RF-SOI CMOS process, occupying a core chip area of only 0.0164 mm^2 (1.5× size reduction compared to state-of-the-art) is demonstrated. The proof-of-concept design has a fractional bandwidth of 71% (21 GHz bandwidth from 19 – 40 GHz) with an insertion loss of 1.19 dB at 30 GHz, and a stopband attenuation of 20 dB at 48 GHz.

V. Future Plans

Since I was awarded the IEEE MTT-S Undergraduate Scholarship, I have started my Ph.D. in the Department of Electrical Engineering at Caltech with a focus on photonic integrated circuits. I am deeply grateful for the support MTT-S community has provided me and look forward to contributing back throughout my Ph.D. and after joining academia as a professor after my Ph.D.

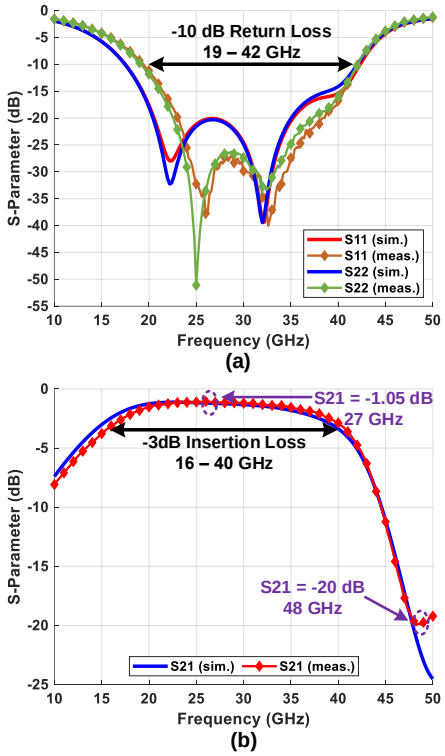

Fig. 3. Measured and simulated scattering parameters of the folded inductor-based mm-Wave BPF. Port definitions are shown in Fig. 2. (a) S11 and S22 parameters showing return loss (b) S21 parameter showing insertion loss.

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