A 60-GHz Vector Modulator in SiGe BiCMOS 5-bit Phase Shifter

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***Abstract*— This paper represents 57-64 GHz 5-bit phase shifter implemented by using vector sum approach. To generate quadrature vectors passive balun and I/Q Network topologies are employed. The desired phase values are obtained by summing reference vectors using VGAs that are controlled by reference currents of control circuitry. The simulated root mean square (RMS) phase error result is 1.85° and the simulated RMS amplitude error result is 0.95 dB at center frequency of 60 GHz. The chip size is 0.33×0.61 mm^2, excluding paths. The power consumption of phase shifter is 19.52 mW where highest insertion value is achieved.**

Keywords—phase shifter, vector modulator, 60-GHz

I. INTRODUCTION

THE RF Phase shifter is one of the sub-level blocks of phased arrays. The scanning resolution of phased arrays is dependent on the number of phase states that are generated by phase shifters. Depending on the application types, phase shifters are divided into two groups active phase shifters and passive phase shifters. Compared to passive phase shifters vector sum topology provides good amplitude & phase control, high integration, high phase resolution and relatively smaller area. However, control circuitry has determining effect on block phase resolution performance, but simulation results demonstrated that phase results are acceptable. The design of the vector modulator phase shifter consists of multiple stages. The purpose and design steps of these stages are described in upcoming sections.

II. CIRCUIT DESIGN

A. Overall Design

The design of the phase shifter consists of multiple stages. These stages are balun, I/Q Network Generator and VGA where RF input is taken by balun then 90-degree phase shifted signals are generated by RC Polyphase filter and VGA stage uses these signals to produce desired phase shift. Fig. 1 presents the block diagram of the vector modulator phase shifter.

B. Marchand Balun Design

The balun has two main purposes in the designs. The first one is impedance matching and the second one is phase shift by providing signal itself and 180-degree shifted signal at the output. Active and Marchand balun are mostly used topologies in literature. The use of the active balun with the vector modulator will increase downside effects of linearity and power consumption, so this topology wasn't considered.

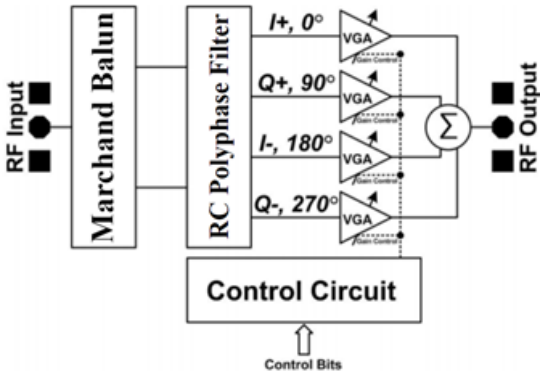

Fig. 1. Block Diagram of the vector-sum phase shifter

Marchand balun topology is chosen to limit power consumption and to have compact design.

C. I/Q Network Generator

The I/Q generator networks are producing 4-signals that have 90-degree phase differences between each other. Different quadrature topologies exist such as RC Polyphase filter, Quadrature All-Pass filter, Lange Couple. The RC polyphase is providing high linearity, compact area and good amplitude-phase balance compared to other topologies. One-stage RC polyphase is used to lower insertion loss and noise figure instead of two-stage. The lowering number of stages affects bandwidth of application but using one stage provides enough application bandwidth at the same time lowered insertion loss. Phase differences between consecutive stages are not exactly 90-degree but insertion loss value tried to be minimized. The usage of a VGA stage can manage these differences by adjusting required current values.

D. Vector Modulator

The working principle of VGA stage depends on control bits and tail current as shown in Fig. 2. Below part of blue dotted line is control circuitry of VGA stage, upper part of red line is vector sum part. The two NMOSs at the very bottom are controlled by control bits for the determination of currents that are used to obtain phase shifts. The four NMOSs above them are used as switches, determination of the quadrature is done by these. The Gilbert Cell topology is used due to its compact area and independence of input drive power. The shunt inductors and series capacitors are providing matching for 50Ω. The shunt resistors provide wide output matching bandwidth. The maximum tail current and number of transistors are chosen to balance performance in terms of both power consumption and insertion loss.

State of Art Comparison	Process Topology	Bandwidth (GHz)	Phase Range Resolution (°)	RMS Gain Error (dB)	RMS Phase Error (°)	Chip Area (mm^2)	Power Dissipation (mW)
[2]	90nm CMOS VSPS	57-64	360 22.5	<0.8	<5.2	0.66	34
[3]	90nm CMOS VSPS	57-64	360 22.5	<1.6	<10	0.61	19.8
[4]	45nm CMOS VSPS	40-67	360 22.5	<1.2	<12	0.51	23
[5]	90nm CMOS VSPS	57-64	360 11.25	<1.8	<10	0.58	31.2
[6]	65nm CMOS STPS+RTPS	57-64	360 11.15	<1.1	<5.5	NA	0
This Work	130 nm SiGe VSPS	57-64	360 11.25	<1.43	<6.9	0.2	19.52

TABLE I. State of Art Values

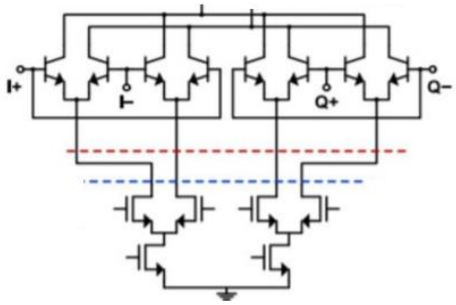

Fig. 2. Block Diagram of VGA Stage [1]

E. Discussion of Results

The design specifications of this sub-block are 5-bit phase shifter which has insertion loss of maximum 10 dB, RMS Phase Error Value of 5.6-degree and RMS Amplitude Error of 1.5 dB. The working frequency range is 57-64 GHz where the center frequency is 60 GHz. The best performance of the phase shifter can be seen around center frequency which is 60 GHz. RMS Amplitude error is less than 1 dB and RMS phase error is less than 2-degree at that frequency. The output matching (S(2,2)) is well below -20 dB around 60 GHz and below -10 dB for a working range of 57-64 GHz. Similarly, input matching (S(1,1)) is below -10 dB through bandwidth. Insertion loss values are around -10 dB which is given one of the given design specifications. To lower insertion loss, maximum tail current can be increased. However, this design aims to achieve less amount of power consumption. At highest insertion loss value, -8.51 dB, power consumption is 19.52 mW which is one of lowest consumption value among other designs in the literature. The overall layout dimensions of the phase shifter sub block are 615 µm × 326 µm which leads to an overall chip area of 0.2 mm^2. The area adjustments are done as mentioned above to achieve very limited chip area consumption.

III. Conclusion

Table 1 compares this vector sum-based phase shifter design with other phase shifter designs around working frequency of 57-64 GHz. The goals of this design were to achieve small area consumption and low power dissipation. Passive balun and I/Q Network generators were chosen to minimize power consumption and active VGA stage was used to better obtain phase resolution. The reference current of VGA stage was chosen to minimize power consumption rather than having higher gain.

IV. Acknowledgment and Career plans

Electrical engineering is one of the fields those small advancements lead to big developments. At the same time, the design process of those small advancements requires high concentration, motivation and encouragement. The IEEE MTT-S Undergraduate/Pregraduate Scholarship motivated and supported me through this design project. I was selected for this award when I was completing my undergraduate at Sabanci University under supervision of Prof. Yasar Gurbuz. Currently, I am pursuing my master's degree at the Georgia Institute of Technology on Electronic Design and Applications track. I am planning to continue my career in corporate life after my graduation.

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