Channel Aggregation Using HRM-based Frequency Interleaving for MM-wave Multi-Gbps Transceivers

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***Abstract*—Recently, channel aggregation has been garnering significant attention at mm-wave and THz frequency bands, enabling multi-Gbps data-rate links.This work explores the use of frequency interleaving data-converters to enable such systems. A harmonic- and image- reject passive mixer has been used to implement a frequency-interleaving channel aggregator, greatly reducing the cost, complexity and power consumption compared to conventional approaches. To validate our claims, we demonstrate a 4-element phased-array transceiver chipset in 45nm RFSOI CMOS, which channelizes 8GHz of bandwidth over 59-67GHz, enabling wireless links with data rates $32Gbps$ and beyond.**

***Index Terms*—channel aggregation, HRM, phased array, transceiver, mm-wave, 60GHz, frequency interleaving, ADC, DAC, wideband.**

I. Introduction

THE ever increasing need for higher wireless data-rates is driving the ongoing research efforts on mm-wave and THz transceivers [1], [2], thanks to the huge unlicensed spectrum available at beyond 60GHz frequency bands. Recently, emerging wireless paradigms such as mm-wave multi-user MIMO [3] and full-duplex systems [4] have been demonstrated successfully, however feasibility of wide-band, power efficient and scalable channel aggregation systems at mm-wave and THz bands are still an open question. The key challenge in achieving several GHz of channel bonded bandwidth necessitates the use of Nyquist rate data-converters whose speed requirement is $\geq 2 \times BW$. Time-interleaving has been popularly used to increase the bandwidth of such data-converters, however they clock jitter and power-hungry buffers [5].The alternative approach is frequency interleaving where the entire input bandwidth is divided into sub-bands and separate low-bandwidth data-converters used to digitize each band. Frequency interleaving not only reduces the system power consumption utilizing low-bandwidth data-converters, but also enables the user to turn-off the sub-converters, as the required BW and data-rate reduces.

In this work, a 60GHz channel aggregation transmitter prototype in 45nm RFSOI CMOS has been demonstrated [6]. In this chipset, 4 channel has been bonded to acheive an operating bandwidth of 59GHz-67GHz, using unique frequency interleaving features of passive harmonic- and image-reject mixers at the baseband.

II. Channel Aggregation Using HRM-based Frequency Interleaving

In the conventional channel aggregation transmitter, an wideband signal is fed into the digital-to-analog converter, which provides the data to a transmitter. The wideband DAC is generally realized using time-interleaving architecture, which suffers from clock jitter, channel mismatch and power-hungry input buffers. As shown in Fig. 1, the main problem of such an architecture is the DAC power consumption increases non-linearly with the sampling rate.

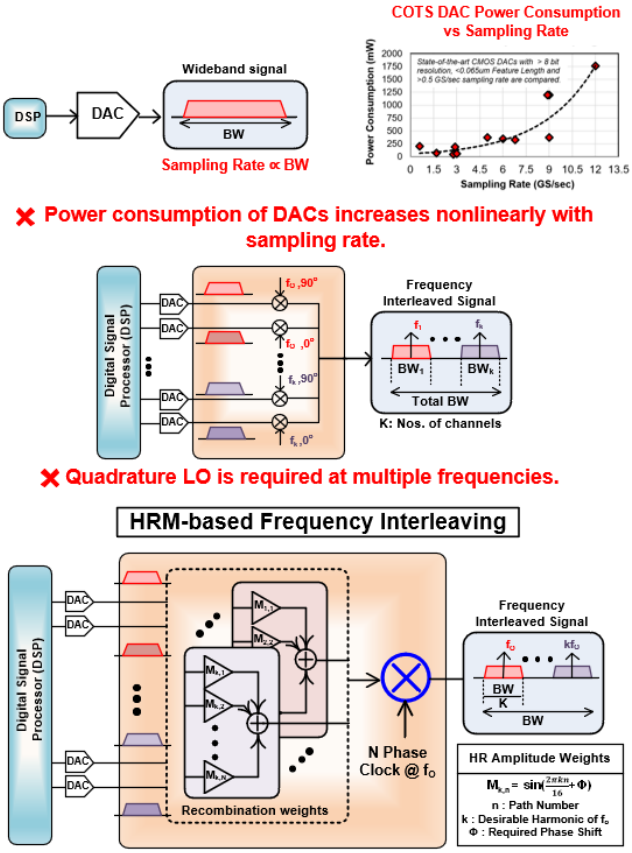

Fig. 1. Conventional Nyquist time-interleaved digitization, frequency-interleaved(FI) digitization and proposed HRM-based architecture FI architecture.

Frequency interleaving(FI) architectures can alleviate this problem and provide an alternative pathway. In prior works, FI has been incorporated to divide the input bandwidth into different sub-bands and a separate lower data-rate ADC/RX block as been used for each of these sub-bands. However, in such a system generation of multiple closely spaced I/Q local oscillator(LO) signals becomes practically challenging [7].

In this work, we use harmonic- and image-reject mixer based channelizer to up-convert the data-inputs to different intermediate IF frequencies and later the IF data inputs are up-

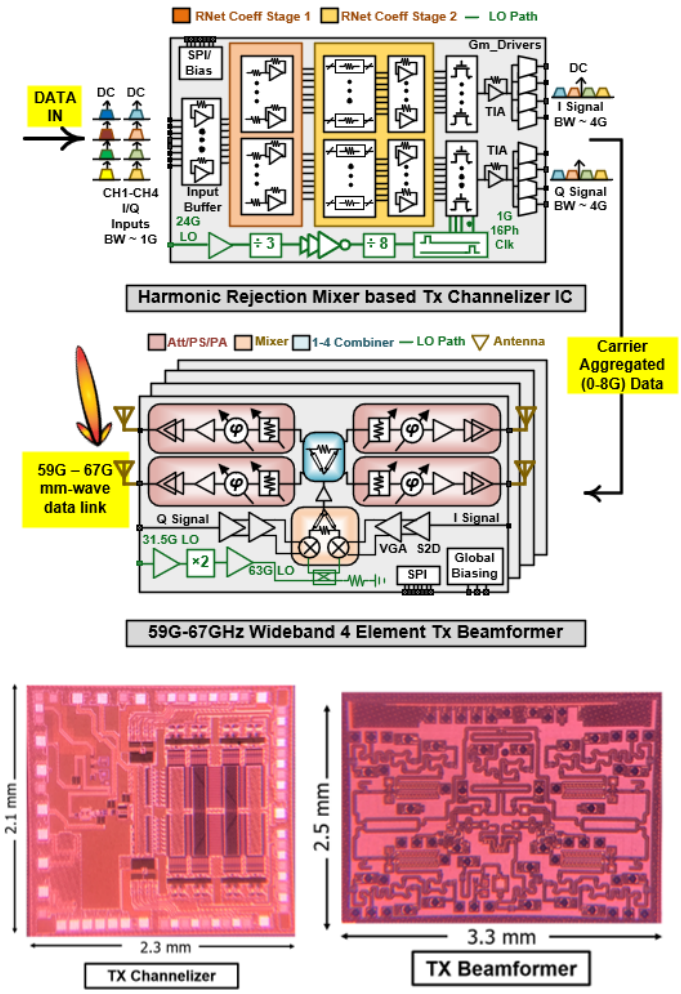

Fig. 2. Block diagram and die photos of phased array transmitter chipset in 45nm RFSOI featuring HRM based FI.

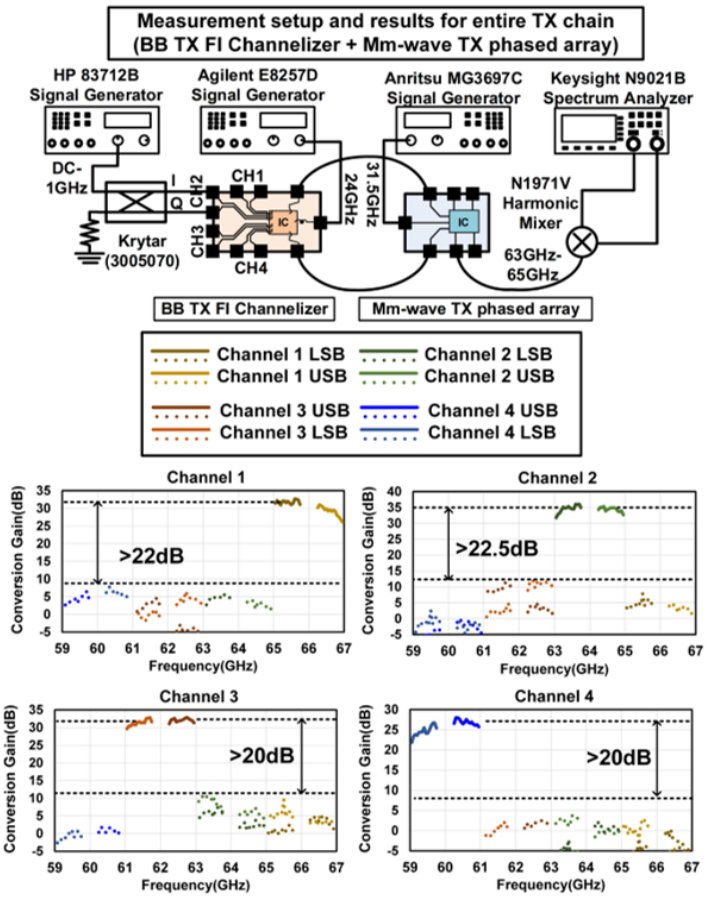

Fig. 3. Measured results for entire transmitter(TX) chain (mm-wave TX phased array + TX BB FI channelizer) are shown.

converted to mm-wave bands using a conventional transmitter beamformer. The key benefit of this architecture is that it uses a single LO frequency for all the intermediate frequency translations. In the baseband IC, we use a passive mixer driven by low-duty-cycle clocks from a single LO and appropriate harmonic recombination weights to synthesize specific harmonics [3] of the LO, while rejecting all other harmonics. Furthermore, these synthesized LO harmonics are used to up-convert 4 channels to appropriate intermediate sub-bands. This same concept can be applied to the receiver(RX) part as well and has been implemented by a few colleagues in our research group.

III. Design and Implementation

Fig. 2 shows the block diagram of the compete transmitter system. Both the 4-channel FI channelizer and 4-element phased-array transmitter has been fabricated using 45nm RFSOI CMOS.The mm-wave phased array TX IC has a bandwidth of 59GHz-65GHz. The IF part of the TX phased array consists of a single-ended to differential equalizer and a variable gain amplifier, followed by a I/Q doubly balanced up-conversion mixer. The mixer output is split into 4path using a series of Wilkinson dividers and drivers. Each phased array element include a transmission-line based phase shifter, reflective attenuator and three stacked-driver and stacked-power amplifier stages. The TX-FI channelizer receives I/Q signals from the DAC for each channel with 1GHz BW at the input. The input signals are scaled using two stages of HR recombination weights followed by a 16-path mixer aggregate all input channels to lie between -4GHz to 4GHz with channels centered at first and third harmonics of the LO, i.e., $+1$GHz, $+3$GHz, -1GHz, and -3GHz. The recombination weights are realized at baseband using TIAs and resistors(R-net), enabling a low-power architecture as shown in [3]. The TX channelizer can drive a 16-element array using four parallel buffers that can each drive a 4-element array IC.

The LO path consists of a 24GHz single-ended LO input that is buffered and fed to a 50% duty-cycle divide-by-three circuit to generate an 8GHz LO, followed by a chain of buffers, divide-by-8 flip-flops and retimers to generate 16-phases of non-overlapping clocks. For mm-wave TX, a 31.5GHz input LO is amplified and fed to a doubler to generate the 63GHz LO.

IV. Measurement Results

Fig. 2 shows the die photos of the baseband(BB) TX FI channelizer and the TX phased array. The chipsets are

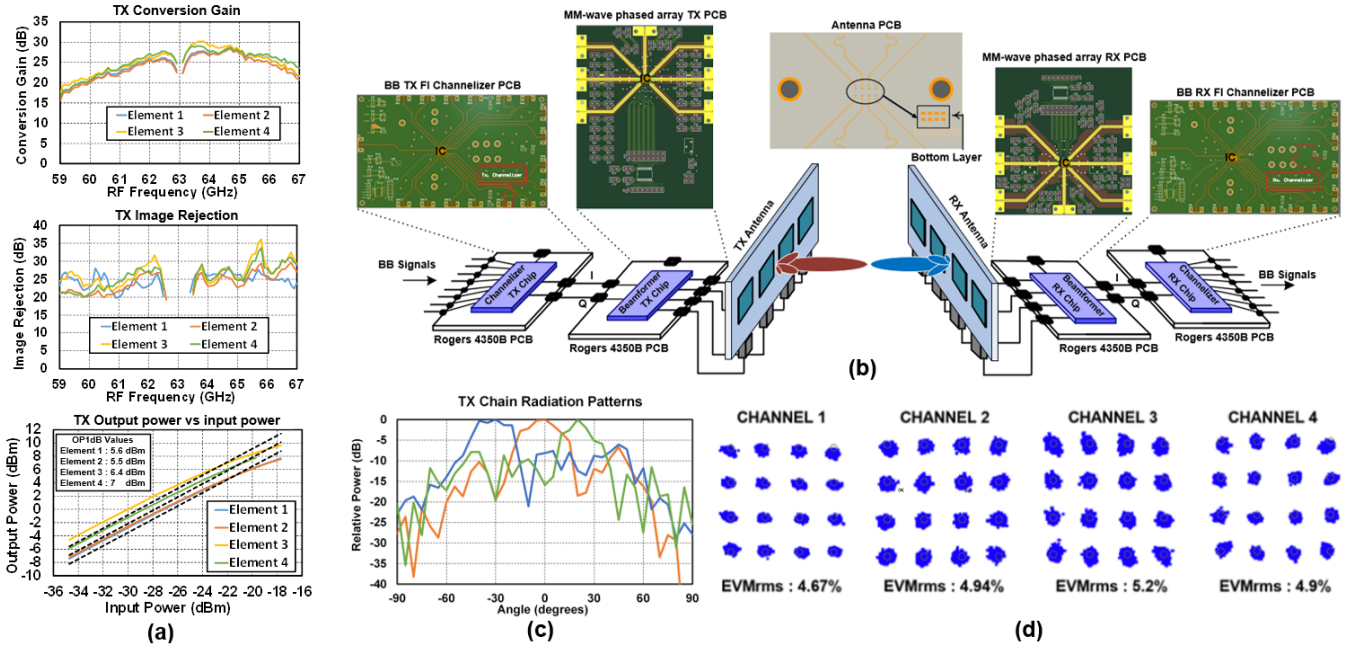

Fig. 4. (a) Conversion gain and linearity of the mm-wave TX phased array IC.(b) Measurement setup for the link measurement. (c) Beam pattern of the transmitter for three different steering angles.(d) EVM results for different channels are shown for 16QAM modulated signals with $100-400$MBaud symbol rates.

fabricated in 45 RFSOI CMOS and consumes an area of $4.83mm^2$ and $8.25mm^2$ respectively.The TX phased array consists of 4-elements. PCB, connector and cable losses are de-embedded from all the measurements reported.

Fig. 3 shows the measured results of the entire TX chain, i.e., while the BB TX FI channelizer is connected to the mm-wave TX phased array. The figure depicts the spurious signals that result from both finite image rejection (IR) and harmonic rejection (HR). A net SNDR of $>$ 20dB (ratio of the desired signal to the sum of all spurs) is computed and reported assuming equal-strength signals in each aggregated channel. Fig. 4(a) shows the performance of the mm-wave phased array TX. Each TX element achieves a IF-RF gain of 20-30dB with an image rejection of 25dB-35dB across 59GHz-65GHz operating frequency range. Ouput linearity measurements show each element can achieve P1dB levels of 5.5-7dBm. Furthermore each element has $>$ 15dB of gain control and $> 360^o$ phase control capabilities to achieve wide-angle beam-steering capability.

Furthermore, this TX chain is integrated with an RX chain with similar architecture. The TX-RX chain is integrated with antenna arrays and measurements are performed in the entire data link. The measurement setup is shown in Fig. 4(b). Fig. 4(c) and (d) shows the results of wireless array pattern measurement and link measurement. An EVMrms $< 5\%$ is measured for each channel, while a $100-400$Mbaud data is applied (currently limited by the signal analyzer capability). Further measurements are ongoing to utilize the entire bandwidth of our chipset, showing an aggregated data rate of $>$ 32Gbps.

V. Career Plan

After my graduation, I would like to pursue a career in industry, to better understand the current needs of the society. I would like to thank Armagan Dascurcu and Ali Binaie, who collaborated with me and equally contributed to the successful completion of the project. Finally, I would like to express my gratitude to the entire MTT-S community for supporting my research giving me the opportunity to attend 2021 International Microwave Symposium.

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