Millimeter-Wave Multi-Mode Frequency Source with Ultra-Wideband and Low Phase Noise in Silicon Technology

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***Abstract*—In this report, we discuss the motivation, main idea, and results of our project that is focused on multi-mode frequency source with ultra-wideband and low phase noise in silicon technology. Firstly, a 2-D mode-switching quad-core oscillator is introduced to obtain four operation modes with a compact chip size. Fabricated in a 40-nm CMOS technology, the oscillator exhibits a 73.2% tuning range from 18.6 to 40.1 GHz. The 1-MHz offset FoM_T is 201.7 dBc/Hz. Secondly, a cascaded mode-switching sub-sampling fractional-N PLL with quadrature dual-mode voltage waveform-shaping oscillator is proposed, which can obtain the merits of high frequency-resolution, low loop noise, and wide frequency locking range. Prototyped in a 28-nm CMOS technology, the proposed PLL exhibits a frequency range from 22.8 to 33.9 GHz. The FoM_j is –236.2 dB.**

***Index Terms*—Cascaded PLL, frequency synthesizer, millimeter-wave, mode-switching, oscillator, quad-mode, sub-sampling, wideband.**

I. Introduction

Millimeter-wave (mm-wave) bands are promising for high data-rate communication, imaging radar, and detection, which require high quality wideband frequency source. Switch techniques are widely developed to expand the tuning range of oscillator. However, the loss of the switches decrease the resonator quality factor greatly. Mode-switching techniques provide solutions to prevent the switch-loss and achieve wide tuning by utilizing oscillators working in different mode without switch in resonators [1]. However, the coupling method of multi-mode oscillator is challenging, and the circuit size is increased dramatically with the increasing of oscillator cores. Therefore, most of the published mode-switching oscillators are dual-mode, which is suitable for ultra-wideband operation at sub-10 GHz but not easy to cover the multiple mm-wave bands. Moreover, to achieve the mm-wave wideband frequency locking, the architecture of phase-locked loop (PLL) still meets challenges.

To address above issues, we have proposed and verified a 2-D mode-switching quad-core oscillator [2], [3] and a cascaded mode-switching sub-sampling fractional-N PLL with quadrature output [4]. Fabricated in 28-nm/40-nm CMOS technology the oscillator obtains the ultra-wide quad-mode tuning range in mm-wave bands, while the PLL achieves high frequency-resolution, low phase noise, low quadrature error, and wide frequency locking range.

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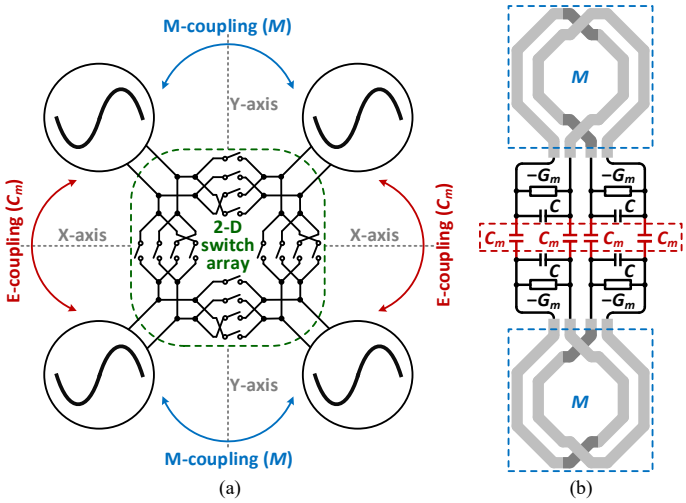

Fig. 1. (a) Architecture of the proposed E-M mixed-coupling quad-mode oscillator. (b) Layout configuration of the oscillator without mode-switch-array.

II. Description of the Project

A. 2-D Mode-Switching Quad-Core Oscillator Using E-M Mixed-Coupling Resonance Boosting

The architecture of the proposed E-M mixed-coupling quad-mode oscillator is shown in Fig. 1(a). The E- and M-coupling are achieved by the coupling capacitor and symmetrically coupled transformer, respectively. By selecting the connection state of the mode-switch-array, both the E- and M-couplings can be excited in even- and odd-modes respectively. Then, four operation modes could be formed. The layout configuration without mode-switch-array is illustrated in Fig. 1(b). Only two resonant tanks are used to form the quad-core oscillator, which is attractive for size-efficient applications. It is notable that, in all of the four modes, four oscillator cores are coupled together and operate simultaneously. Thus, the phase noise improvement from the multi-core structure could be obtained in the four-mode operation. Meanwhile, the digitally controlled tail-resistor array is used to optimize the flicker noise up-conversion in the quad-mode frequency range. The oscillator is fabricated in a 40-nm CMOS technology. The micrograph of the chip is shown in Fig. 2. The measured results exhibit a 73.2% tuning range from 18.6 to 40.1 GHz. The best phase noise at 1 MHz offset is –108.5 dBc/Hz, corresponding to a FoM of 184.4 dBc/Hz and FoM_T of 201.7 dBc/Hz. The variation range of FoM over the whole frequency range is 3

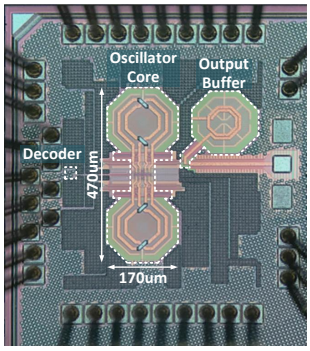

Fig. 2. Chip micrograph of the 2-D mode-switching quad-core oscillator.

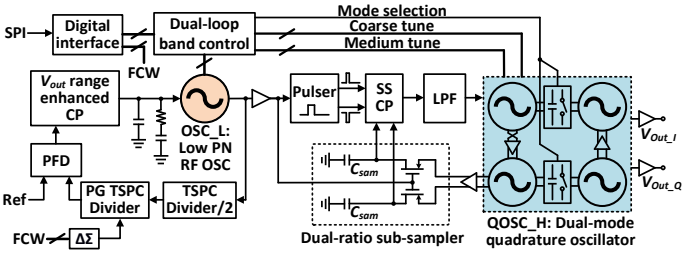

Fig. 3. Architecture of the cascaded mode-switching sub-sampling fractional-N PLL with dual-mode quadrature oscillator.

dB. The $1/f^3$ phase noise corner is 220 to 620 kHz.

B. Cascaded Mode-Switching Sub-Sampling Fractional-N PLL with Quadrature Output

A cascaded mode-switching sub-sampling fractional-N PLL with dual-mode voltage waveform-shaping oscillator is proposed. The block diagram is shown in Fig. 3. The proposed PLL consists of a type-II PLL cascaded with a divider-less mode-switching sub-sampling loop. Thus, the structure has the merits of robust frequency control and low loop noise. Moreover, the mode-switching mechanism can support the wide frequency locking range without divider in the sub-sampling loop. Fig. 4 shows the frequency diagram of the multi-ratio sub-sampling PLL for frequency multiplication. Each possible integer ratio sub-sampling PLL can lock to (i.e., ratio of N, N+1...) can fully cover one corresponding mode of the multi-mode oscillator. Thus, the entire wideband mm-wave bands can be fully locked. Both oscillators are designed as digitally-voltage controlled oscillator. Then, the tuning range of each oscillator is divided into multiple sub-bands. For a certain sub-band of the low frequency oscillator, the corresponding sub-sampling locking range doesnt overlap, and only one sub-sampling ratio is feasible. A quadrature dual-mode voltage waveform-shaping oscillator is utilized in the mode-switching sub-sampling loop to achieve the low phase noise and wide tuning range, simultaneously. Compared with conventional quadrature oscillator, the dual-mode quadrature topology can achieve lower phase noise and phase error. The cascaded mode-switching PLL is implemented in a conventional 28-nm CMOS technology, as shown in Fig. 5. The proposed PLL exhibits a frequency range from 22.8 to 33.9 GHz. The phase noise across the frequency band is from –104.1 to –108.2

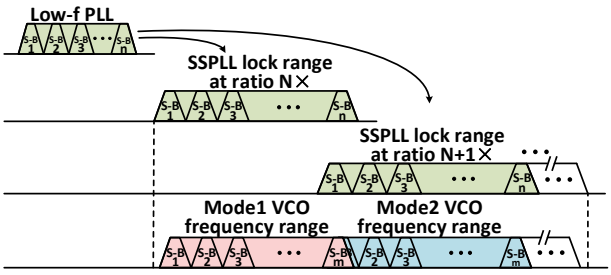

Fig. 4. Frequency of the proposed multi-mode sub-sampling PLL.

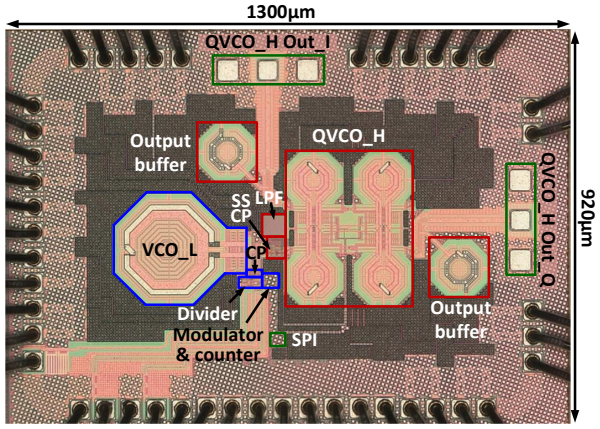

Fig. 5. Chip micrograph of the cascaded mode-switching sub-sampling fractional-N PLL.

dBc/Hz at 1 MHz offset. The measured quadrature phase error is 0.5° to 1.2°. With a reference of 52 MHz, the jitter $\mathrm{FoM_j}$ is –236.2 dB. Compared with PLLs using high frequency crystal, the system cost is reduced.

III. Fellowship Impact and Career Plan

I am honored and grateful to receive the recognition of IEEE Microwave Theory and Technique Society for the 2020 Graduate Fellowship Award in support of my research work. It was a great motivation to continue my research and obtain a valuable research experience. The award also provided an opportunity to attend International Microwave Symposium 2020 and meet the best researchers across the globe working on cutting-edge technology. I plan to continue my research after graduation to further develop the mm-wave and terahertz wireless systems in either industry or academia.

References

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