A wideband, high output power amplifier from W-band and above

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***Abstract*— This manuscript describes the research results undertaken under the 2020 IEEE MTT-S Graduate Fellowship. In particular, a new gain boosting technique is developed and implemented in a 60 to 145 GHz distributed amplifier (DA) in an Indium Phosphide (InP) process. The measured results demonstrate a 4-dB gain improvement through out the band. The amplifier has a maximum saturated power (P_{sat}) of 20.9 dBm at 75 GHz with the measured 1-dB compression power (P_{1dB}) of 18.5 dBm. The dc power consumption is 440 mW and chip size of 1.6 mm × 0.6 mm. The similar gain boosting technique is implemented with a 4 to 1 power combiner in the band of 110 to 170 GHz also in InP process. The fabricated chip size is 2.8 × 1.8 mm.**

***Index Terms*— 6G, bandpass, distributed amplifier (DA), feedback, gain boosting, heterojunction-bipolar-transistor (HBT), Indium Phosphide (InP), millimeter-wave (mmW), wideband.**

I. Introduction

WIDEBAND, high gain, high output power, and low power consumption are the prominent figures of merit for high data rate communication systems, high-resolution radars, and instrumentation applications [1]. When frequency emerges to the millimeter-wave (mmW) and sub-millimeter-wave regions, maintaining high gain and output power becomes challenging due to increased transmission line losses, unwanted couplings, and parasitic elements [2], [3]. Gain is further degraded when a transistor operates near the transition frequency (f_T) for a given process. Distributed amplifiers (DAs) have been proven to offer ultra-wideband performance, but still suffer from gain-bandwidth (GBW) trade-offs [1].

Different techniques have been reported to enhance the DA gain, including cascaded gain stages, cascaded multi- and single-stage and matrix DAs. However, the results come along with larger chip sizes and higher dc consumption. These techniques also increase the gain in a multiplicative amplification, thereby degrading stability. Cascaded amplifiers also reduce the bandwidth performance depending on the number of cascaded stages and passive losses. Furthermore, mismatches between the stages introduce mid-band ripples and worsen the group delay of the amplifier [1].

In this report, we present a new bandpass distributed amplifier using an inductive feedback technique to uniformly enhance the gain for the entire passband while maintaining the upper cut-off frequency [2]. To validate the proposed technique, a 60 – 145 GHz bandpass DA is designed and fabricated in an Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) process. The prototype exhibits a measured average small-signal gain of 10.5 dB, a 3-dB bandwidth from 60 – 145 GHz, and a maximum saturation power (P_{sat}) of 20.9 dBm with the corresponding 1 dB compression power (P_{1dB}) of 18.5 dBm at 75 GHz. The feedback DA has a 4-dB gain improvement spanning from 64 to 142 GHz compared to its counterpart conventional DA. In addition, similar technique is applied in the band of 110 to 170 GHz along with a 4:1 power combiner is presented. The chip is also fabricated in an InP process. The chip size is 2.8 × 1.8 mm.

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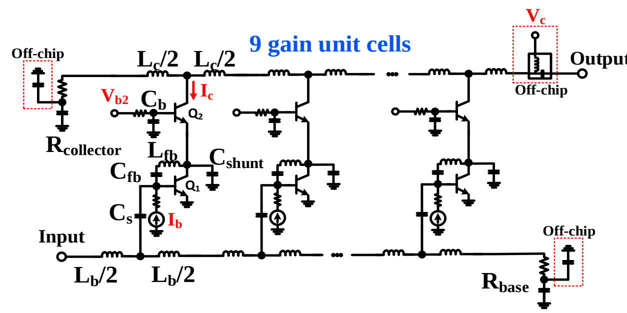

Fig. 1. The proposed bandpass inductive feedback DA

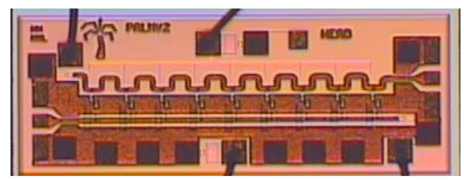

Fig. 2. Chip photograph of the proposed inductive feedback bandpass DA with a die size of 1.6 mm x 0.6 mm.

II. Proposed Gain Boosting Technique

We propose a wideband gain enhancement technique for a DA, which provides a high roll-off bandpass structure by using an inductive feedback network applied to a double-stacked gain cell, as shown in Fig. 1. The proposed technique introduces a feedback inductor L_{fb} and a shunt capacitor C_{shunt} at the collector of the common emitter transistor in the stacked-HBT gain cell configuration. The feedback inductor L_{fb} introduces gain peaking at the low-frequency edge while the shunt capacitor C_{shunt} boosts up the gain at the high-frequency edge. The feedback capacitance C_{fb} acts as a dc block from the collector to the base of transistor Q_1 to prevent shorting out the HBT.

Fig. 1 shows a nine-stage DA employing the proposed gain cell. in addition to a commonly used series input capacitor C_s to obtain a high bandwidth. In general, the feedback network has an insignificant impact on the overall input capacitance of the gain cell for most of the passband. The input capacitance of the feedback gain cell is then approximately equal to C_{be1}. The coupling capacitor C_s factors the gain of the DA by the capacitive division ratio, M, defined as $M = C_s/(C_s + C_{be1})$. In order to maximize the bandwidth, the ratio M can be much smaller than one. Fig. 2 shows the die photo of the proposed feedback DA.

III. Experimental Results

Fig. 3(a) shows the measured and simulated S-parameter of the feedback DA. The proposed gain boosting feedback DA

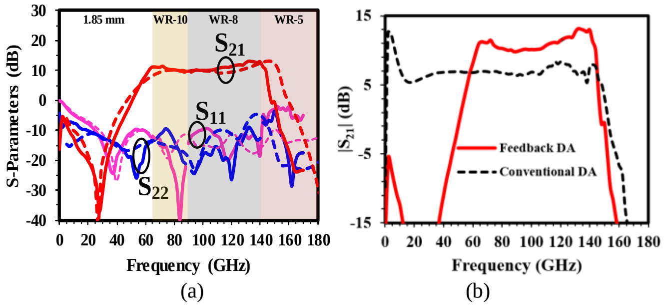

Fig. 3. (a) Measured (solid) and simulated (dashed) S-parameters of the proposed feedback DA and (b) S_{21} of the proposed DA and the conventional low-pass DA.

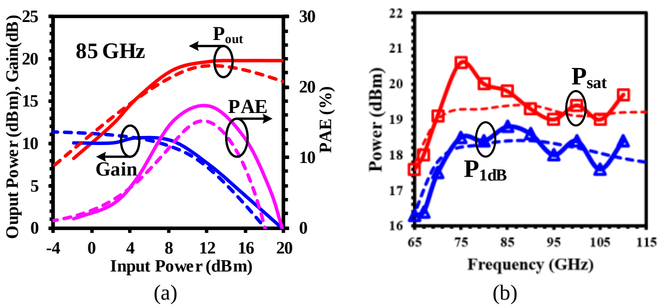

Fig. 4. (a) Measured and simulated output power, gain, and PAE of the proposed feedback DA at 85 GHz and (b) P_{sat} and P_{1dB} over the frequency of the feedback DA. The solid line and dashed line are measurement and simulation, respectively.

exhibits an average gain of 10.5 dB with a positive gain slope. The 3-dB bandwidth extends from 60 GHz up to 145 GHz, making the gain-bandwidth product of 285 GHz. The DA achieves input and output return loss better than -10 dB up to 110 GHz. The transmission zero appears at 27 GHz. Fig. 3(b) illustrates the measured gain S_{21} of the feedback DA. An average gain improvement of 4 dB is achieved in the feedback DA compared to the conventional DA from 64 to 142 GHz.

Fig. 4 presents the large-signal measurement of the proposed feedback DA. At 85 GHz from Fig. 4(a), the DA attains a saturated power (P_{sat}) of 19.8 dBm, a 1-dB compression output power (P_{1dB}) of 18.8 dBm, and a maximum power added efficiency (PAE) of 17.3 %. The measured results at these frequencies are slightly higher than the simulated ones. This effect might be caused by the conservative modeling of the device. The input power is driven up to 20 dBm without damaging the device. The output signal of the DA at high input power is observed with the spectrum analyzer. There are no indications of parametric instability. The measured and simulated 1-dB compression output power, P_{1dB}, and the saturated power, P_{sat}, over the frequencies are provided in Fig. 4(b). The maximum achievable P_{sat} is 20.9 dBm at 75 GHz with the corresponding P_{1dB} of 18.5 dBm.

IV. Four to One Power Combined Amplifier

With the proof-of-concept gain boosting technique illustrated from 60 to 145 GHz, the similar technique is implemented in 110 to 170 GHz bandwidth. To achieve a higher output power, a 4:1 power combiner using Lange coupler is implemented. The unit power amplifier cell is a 9-stage DA with inductive gain boosting feedback technique. Fig. 5 shows the die photo of the

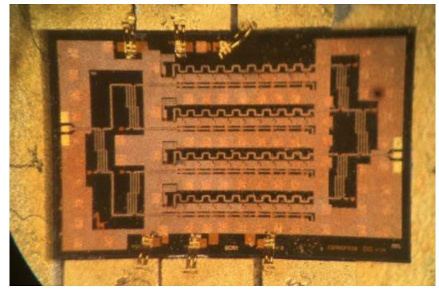

Fig. 5. The proposed 4:1 power combined DA. The chip size is 2.7 × 1.8 mm

fabricated power amplifier. The chip size is 2.7 × 1.8 mm. The simulated 3-dB bandwidth of the amplifier covers from 100 GHz to 180 GHz. The maximum simulated P_{sat} is 24 dBm.

V. Conclusion

A wideband gain boosting technique for distributed amplifiers has been introduced and analyzed. The technique employs an inductive feedback network to achieve a wideband gain improvement without sacrificing the gain-bandwidth product. Compared to the conventional DA, the proposed gain enhanced DA exhibits an average gain improvement of 4 dB over a wide bandwidth from 64 to 142 GHz. More importantly, the gain enhancement is achieved without a trade-off in gain bandwidth, dc power consumption, output power, and chip size.

VI. Future Work

The fabricated power combined DA in Fig. 5 will be characterized and documented. Further modification and adjustment might be essential to further improve the performance of the amplifier. Higher waveguide band where the gain falls short can be considered to implement the technique.

VII. Career Plan and Impact Statement

I am currently completing my doctorate dissertation and preparing for graduation. I will join the industry in Santa Clara, California in the summer as a Senior Design Engineer. I am truly honored to receive the 2020 IEEE MTT-S Graduate Fellowship. I deeply appreciate this prestigious award from the MTT-Society. Although I did not have the chance to attend the IMS 2020 due to the pandemic, it is still a great chance for me to talk and discuss with other fellow recipients. The opportunity has provided me with great technical knowledge and new colleagues around the world.

Acknowledgment

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Reference

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