Final Project Report

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***Abstract*—Signal Integrity – Power Integrity (SI-PI) co-analysis becomes essential as systems move towards system-critical conditions. It is crucial to optimize the channel for its best performance and to find the controllable parameter enablers. However, computational cost of precision modeling of PI and SI structures is very high, making direct application of traditional optimization methods prohibitive. This project aims to apply numerical optimization techniques to develop an advanced optimization methodology for modeling and design of coupled signal and power integrity analysis of high-speed interconnects and power delivery networks, with high precision and low computational cost.**

***Index Terms*— modeling, noise control, optimization, power delivery network, power integrity, signal integrity**

I. Introduction

Signal Integrity (SI) addresses two major concerns in electrical design: timing and the quality of the signal, and typically studies waveform distortions. Power Integrity (PI) addresses voltage variations in the power/ground network due to noise, and can impact timing, signal quality, and functionality. The traditional methodology relies on the assumption that Signal and Power Integrity are two separate problems when analyzed for channel budget. Signal Integrity analysis considers an ideal power delivery system. However, simultaneous switching output noise (SSO) and buffer behavior is not linear, and the interaction between signal network and Power Delivery Network (PDN), at chip, package, and PCB, influences the eye voltage/timing margin at the receiver. Furthermore, systems are moving towards system-critical conditions as we move towards the hundreds of Gigahertz, and it is becoming crucial to optimize the channel for its best performance and find the controllable parameter enablers, if there are any; Signal Integrity - Power Integrity (SI-PI) co-analysis becomes essential now. Furthermore, Computational cost of precision modeling of PI and SI structures is very high, making direct application of traditional optimization methods prohibitive.

II. Towards SI-PI co-analysis

The design process of power delivery networks (PDN) in modern computer platforms is becoming more relevant and complex due to its relationship with high-frequency effects on signal integrity. When the signals at different on-board modules of a PDN start switching, they cause current surges that create voltage noise on the pads of the on-board modules, introducing high-frequency components. If this voltage noise is not controlled, it can cause the amplitude of the eye diagram in the vertical direction to collapse [1]. Additionally, the signal flowing to a reference plane will increase skin and proximity effects (due to the high-frequency components), increasing jitter due to dispersion and further reducing the eye opening. This leads to functional failures in the computer platform as internal core circuits suffer setup- and hold-time errors. Some of these common problems can be mitigated by using decoupling capacitors.

Our work focuses on a numerical optimization approach to determine the number of decoupling capacitors in a PDN, aiming at decreasing the number of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency domain and the transient voltage droop in the time-domain.

III. Power Delivery Network Model

In our work we consider the PDN of a CPU power net of an Intel® Xeon server platform, as shown in Fig. 1. The yellow section is the power delivery network under study, while other colors represent signal networks. The PDN structure can be modeled in a limited frequency band using a simple lumped RLC circuit. Using parameter extraction techniques, we obtained the lumped model extracted from the PDN layout [2] shown in Fig. 2.

IV. Optimization of a PDN Combining Frequency- and Time-Domain Effects

We optimize the number of decoupling capacitors using as design specifications a maximum target impedance of 2.24 mΩ, a minimum target impedance of 1.02 mΩ, and a minimum voltage specification of 0.8 V for the transient voltage pulse. The optimization problem uses a minimax formulation, and we use the Nelder-Mead optimization algorithm to solve the problem. The results of our work are published in [3].

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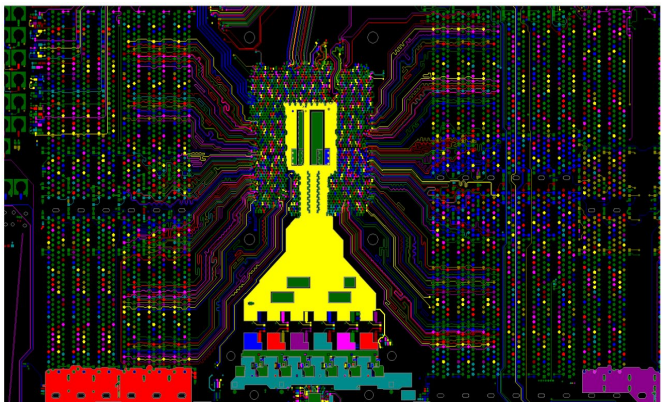

Fig. 1. Power delivery network (PDN) layout of an Intel® Xeon® platform [3].

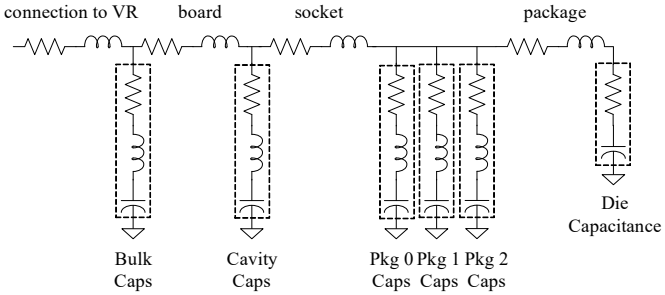

Fig. 2. Lumped equivalent circuit of the power delivery layout schematic of Intel® Xeon® platform [3].

V. Conclusions

We used several different initial number of capacitors for each type of capacitor used and we found successful results in meeting the maximum impedance and minimum transient voltage specifications, with no more than 152 capacitors in total. We also found that when using an ideal voltage regulator, the Bulk capacitors did not have a significant impact on the PDN response. We found that by limiting the maximum total number of capacitors allowed, we obtained a more robust formulation, capable of minimizing the number of capacitors to yield a PDN that satisfies the target impedance and minimum transient voltage supply specifications.

VI. Next Career Plans

The MTT-S Fellowship has allowed me to focus full time on the PhD research. I have also been teaching an undergraduate course at the university where I am studying, and once I finish my PhD I plan on staying as an adjunct professor until I can become part of the full time faculty. This will allow me to continue my research work which would not be possible if I went back to the industry.

VII. Impression about having attended the IMS 2020

IMS 2020 was scheduled to take place in Los Angeles, California, however due to the COVID-19 pandemic the event took place virtually. I look forward to attending an in-person IMS when the pandemic allows it. I am especially looking forward to the Three Minute Thesis Competition as I think this is a great way to cultivate presentation and research communication skills. Hopefully there could be a future small scholarship for the MTT-S Fellowship awardees so we can attend the next IMS that will be help in-person.

References

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