A Reconfigurable L/X Band PLL-Less Ultra-Low-Noise Frequency Synthesizer for 5G

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***Abstract*— This document reports on the research undertaken during the past year under the support of the MTT-S Graduate Fellowship. We present an 8.6 GHz oscillator utilizing the third-order antisymmetric overtone (A_3) in a lithium niobate ($LiNbO_3$) radiofrequency microelectromechanical systems (RF-MEMS) resonator. The oscillator consists of an acoustic resonator in a closed loop with cascaded RF tuned amplifiers (TAs) built on TSMC RF GP 65 nm CMOS. A frequency divider chain for a ~1.1 GHz output was also implemented. The phase noise performance of both the *X* and the *L* band outputs surpasses the state-of-the-art (SoA). The demonstrated performance shows the strong potential of microwave acoustic oscillators for 5G frequency synthesis.**

***Index Terms*— lithium niobate, MEMS, oscillator, phase noise.**

I. Introduction

CURRENTLY, the sub-3 GHz frequency bands are too congested to meet the ever-increasing data rates demanded by many cellular users. The call for higher bandwidths has pushed the 5G radios towards mm-wave frequencies. Apart from larger bandwidth, 5G transceivers are expected to feature higher sensitivity and selectivity while producing longer battery life; all in small form factors. To achieve all the above seamlessly, frequency synthesizers must be revolutionized on architecture, circuit, and device levels. To relax the requirements on the sensitivity and selectivity of the RF front-end for 5G, the synthesizer phase noise has to be reduced via a non-conventional way. One key challenge in implementing high-performance chip-scale synthesizers for 5G beyond 6 GHz lies in the lack of high-performance miniature resonators that can enable signal generation with minimal phase noise and power consumption.

State-of-the-art (SoA) microwave oscillators are based on LC, microstrip, active, and dielectric resonators (DR). On-chip lossy LC tanks are compact, hence offering a low-cost solution. However, their low *Q* at microwave frequencies translates to poor phase noise and high-power consumption. DROs offer superior phase noise performance, but they are bulky and consume a large amount of power. Alternatively, oscillators based on RF-MEMS resonators that harness the confinement of acoustic waves and have the size of hundreds of microns, are attractive for portable devices. Recently, acoustic resonators with resonances above 10 GHz have been demonstrated in different platforms such as aluminum nitride (AlN) thin-film bulk acoustic resonators (FBARs), AlN contour mode resonators (CMRs), ferroelectric resonators, FinFET resonators, and lithium niobate ($LiNbO_3$) resonators. From this group,

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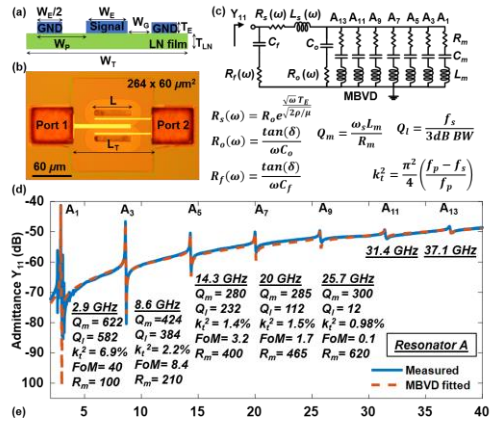

Fig. 1. (a) Mockup cross-sectional view of the resonator. (b) Optical image of the fabricated resonator. (c) Measured and MBVD fitted response for the first 5 odd modes. (d) Multi-resonance equivalent MBVD model.

$LiNbO_3$ resonators feature the highest demonstrated figure-of-merit ($FoM_{RES} = Q \times$ electromechanical coupling coefficient, k_t^2) making them the more suitable candidate for enabling chip-scale oscillators with simultaneously low phase noise and low power consumption [1]-[3].

With access to the above microwave resonators, the next challenge is to design the oscillator or the frequency synthesizer. Conventional frequency synthesis has been relying on a power-hungry phase-locked loop (PLL) referenced to a bulky high *Q* crystal oscillator (XO). XOs are hardly tunable and generate only low frequencies (<120 MHz), thus necessitating a PLL as a tunable frequency multiplier and leading to a larger footprint. To overcome these shortcomings, we develop a direct frequency synthesizer based on integrating an X-band $LiNbO_3$ RF-MEMS oscillator with CMOS open-loop frequency dividers. Instead of generating the local oscillator (LO) frequencies from a low-frequency source and "bubble up" through a PLL, our work creates a low-power microwave low noise source and then "trickle-down" to an LO frequency range from X to L bands via the frequency division. Our approach has the following vital benefits: (1) lower power consumption; (2) a smaller footprint when compared to off-chip XOs/PLLs; (3) RF carriers with lower phase noise/jitter for better receiver sensitivity; (4) spurs-free phase noise (unlike PLL) for enhancing receiver selectivity; and (5) a faster response and lower energy dissipation from removing the overhead for XO startup or a PLL locked to an XO.

The rest of the paper is organized as follows: Section II reports on the design, implementation, and measurement results of the synthesizer. Finally, Section III focuses on my career plans.

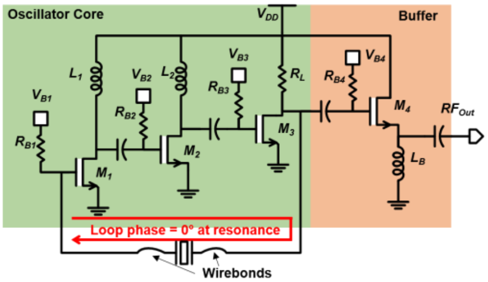

Fig. 2. Schematic of the 8.6 GHz oscillator core and buffer.

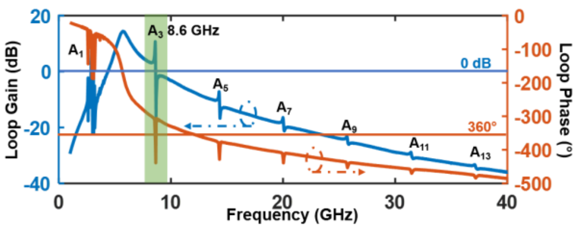

Fig. 3. Post-layout simulated loop gain and phase.

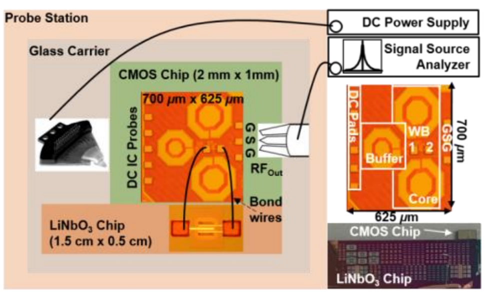

Fig. 4. Measurement setup.

II. Frequency Synthesizer

A. Antisymmetric Mode $LiNbO_3$ RF-MEMS Resonators

Antisymmetric modes are a class of Lamb-wave modes characterized by their antisymmetric vibrations about the median plane of the plate. The resonance of an A-mode resonator is largely set by the thickness of the $LiNbO_3$ film (T_{LN}) and the mode order. A smaller thickness would translate to a higher fundamental frequency; however, this needs careful fabrication and a sophisticated deposition method for thin films to maintain high *Q*. The overmoding approach helps in achieving higher resonant frequencies without thinning down the resonator and adding fabrication complexity. It also provides better linearity and power handling due to the larger volume of the device structure. The resonator structure is shown in Fig. 1.

B. X- Band Oscillator

As shown in Fig. 2, three inverting stages are adopted for our oscillator to excite A_3. The first and second stages are inductively loaded NMOS CS tuned amplifiers (TAs). The third is a wideband resistive loaded NMOS CS stage that can operate as an amplifier or an attenuator by varying the gate voltage. The TAs bandpass response is determined by the loading inductors (L_1 and L_2). The inductance values are chosen for a gain peak at 5.7 GHz, a frequency between A_1 (2.9 GHz) and A_3 (8.6 GHz). This bandpass response excites A_3 and suppresses A_1 and higher-order resonances as shown in Fig. 3.

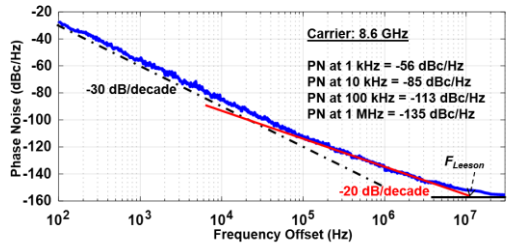

Fig. 5. Measured phase noise of the 8.6 GHz carrier.

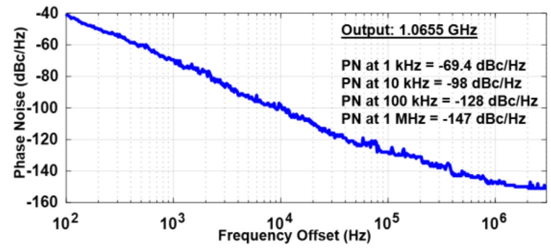

Fig. 6. Measured phase noise of the 1.07 GHz output.

The TSMC RF GP 65 nm CMOS chip is integrated with the MEMS chip on a glass substrate via wire bonding. The CMOS circuitry occupying an area of 700 μm × 625 μm is integrated with the resonator as shown in Fig. 4. The oscillator achieves a measured phase noise of -56, -113, and -135 dBc/Hz at 1 kHz, 100 kHz, and 1 MHz offsets from an 8.6 GHz carrier while consuming 10.2 mW. A phase noise plot is shown in Fig. 5.

C. L- Band Output

The X-band oscillator is followed by a single-ended-to-differential output stage for conditioning the signals before entering the frequency divider. The frequency dividers used are simple current mode logic (CML) dividers that operate with moderate input and output swings and very high speeds in submicron CMOS. A divide-by-8 circuitry is needed to convert the 8.6 GHz RF-MEMS output to 1.1 GHz output. The total dc power consumption of the L-band circuitry is 12 mW, where the oscillator consumes 6.9 mW and the dividers consume 5.1 mW. The synthesizer achieves a phase noise of -69.4 and -147 dBc/Hz at 1 kHz and 1 MHz offsets, respectively, from a 1.07 GHz output. A phase noise plot is shown in Fig. 6.

III. Career Plans

After completing my PhD this spring, my plan is to start joining the Industry world, working on exciting projects related to RF frontend (RFFE) wireless chips for 5G, and Wi-Fi.

References

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