Design of High-Performance Multiband Millimeter-Wave Integrated Frequency Synthesizer and Phased-Array Transceivers for 5G Communications

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***Abstract*—In this report, we will present two high-performance multiband millimeter-wave multi-ratio frequency multipliers that cover the frequency bands from 24 to 40 GHz. The inputs of these frequency multipliers are low-frequency and narrowband signals that can achieve low phase noise performance in silicon, while they can generate high-frequency and wideband output signals without phase noise degradation. We use high-efficient nonlinear devices to generate harmonic currents, and adopt the injection-locking technique and tunable fourth-order resonator to select the desired harmonic and reject undesired signals. The proposed frequency multipliers achieve 55.5-fs jitter and 57.7-dBc harmonic rejection.**

***Index Terms*—Bandwidth extension, frequency multiplier, injection-locked, LO generation, millimeter wave, phase noise.**

I. Introduction

Multiband communications at millimeter-wave (mm-wave) frequency range have attracted more attention, especially at frequencies from 24 to 42 GHz for the fifth-generation (5G) communication. However, such kinds of wideband high-frequency systems have stringent requirements on local oscillators (LO), which must have sufficient low phase noise property. To solve this problem, people tend to use frequency multiplier to generate mm-wave signals. Therefore, the great phase noise performance in low-frequency sources can be utilized. However, when conducting this method into wideband systems, the low-frequency input sources also meet the wideband requirement, which will influence their phase noise. Thus, multi-ratio frequency multipliers become a new solution to extend the bandwidth. In this project, we will present two multi-ratio injection-locked frequency multipliers (MR-ILFM). The first design achieves $\times 3.5$, $\times 4.5$, and $\times 5.5$ three different multiplication ratio and realizes 21.7-to-41.7-GHz output frequency ranges. While the second design achieves $\times 5$ and $\times 7$ frequency multiplication with a 22.4-to-40.6-GHz frequency range.

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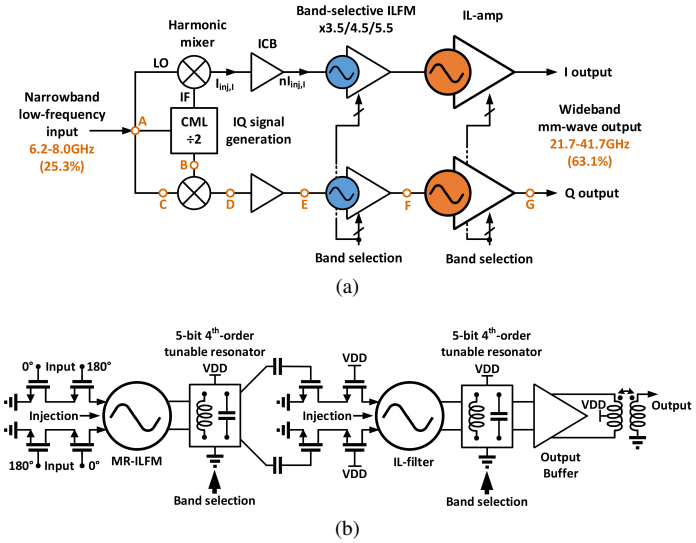
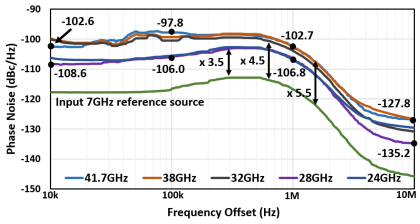


Fig. 1. System architecture of (a) the first and (b) the second designs.

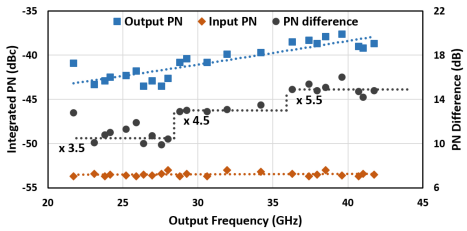
II. Multi-Ratio Injection-Locked Frequency Multiplier

The concept of MR-ILFM is to use a high-efficiency harmonic generator based on the nonlinear property of transistors to generate a comb-like current with multiple harmonics. Then, inject the current into an oscillator with a tunable load. Thus, the injection-locked oscillator will lock to one of the harmonics which is determined by the resonance property of the tunable load, and rejects other harmonics. By tuning the load of the oscillator, one can simply change the harmonic tone to be locked and thus change the multiplication ratio. Due to the property of the wide locking range ILFM, the output phase noise of MR-ILFM will not degrade, and the undesired harmonics will be rejected by injection locking and the filtering property of the load.

The first proof-of-concept is a 21.7-to-41.7-GHz MR-ILFM, as shown in Fig. 1(a) [1]. This work aims at generating quadrature signals, so we use a frequency divider at the input to generate quadrature signals, and mix these signals with the original input through a harmonic mixer to generate harmonics at $\times 3.5$, $\times 4.5$, and $\times 5.5$. Besides, these harmonics are injected into the ILFM through an injection-current boosting (ICB) transformer [2], and a switchable capacitive-coupled

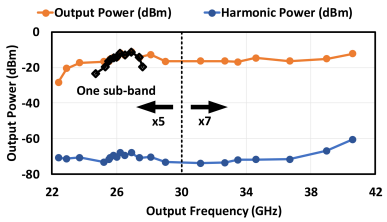


(a)

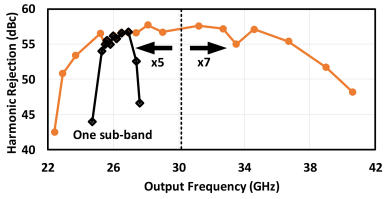


(b)

Fig. 2. (a) Measured phase noise plot, and (b) measured phase noise comparison of the input and the output signals in the whole frequency bands of the first design.



(a)



(b)

Fig. 3. (a) Measured output power, harmonic power, and (b) harmonic rejection over operating frequencies of the second design.

fourth-order resonator forms the load of the ILFM to extend the locking range [3] and increase the tuning range. An injection-locked amplifier (IL-amp) is followed by the MR-ILFM to further suppress the undesired harmonics using the harmonic rejection property of the injection-locking technique [4].

The second proof-of-concept is a 22.4-to-40.6-GHz MR-ILFM, as shown in Fig. 1(b) [4]. This work aims at high harmonic rejection. This time, a high-efficient injection structure is adopted by using stacked transistors. The stacked transistors are driven by differential signals such that they can generate a chopped current which contains multiple high-frequency harmonics with a very low dc current. The generated current then injects into core oscillator with capacitive-coupled tunable fourth-order load to realize frequency multiplication. By selecting the fifth or the seventh harmonic, this MR-ILFM realizes $\times 5$ and $\times 7$ multiplication ratio. To further improve the harmonic rejection, we cascade another MR-ILFM with the same structure. And the second MR-ILFM acts as a filter with the multiplication ratio of one, so that we name it as the injection-locked filter (IL-filter). An output buffer is then connected for testing.

III. Measurement

Both two chips are fabricated in the 65-nm CMOS process. The first one consumes 74.4 mW power under a 1.2 V supply and occupies a 0.52 mm^2 area. The input frequencies are from 6.0 to 8.2 GHz. Fig. 2(a) gives the measured phase noise plot at frequencies of 24, 28, 32, 38, and 41.7 GHz together with the phase noise from the input source at a frequency of 7 GHz as the reference. The MR-ILFM achieves -105.6 dBc/Hz PN at 100 kHz offset and -42.7 dBc integrated phase noise (from 1 kHz to 100 MHz) at 24 GHz. The PN differences between input and output signals are around 10.8, 13.1, and 14.8 dB with the multiplication of $3.5\times$, $4.5\times$, and $5.5\times$ through all frequency bands as shown in Fig. 2(b), which are close to the theoretical values.

The second chip is excited by an on-chip VCO with a frequency range from 4.3 to 5.8 GHz. The MR-ILFM and IL-filter consume 10.0-mW power under 1-V supply, and the output buffer consumes 5.4-mW power. Fig. 3 shows the measured output power, highest harmonic power, and worst harmonic rejection across the whole frequency band. A harmonic rejection of more than 50 dBc is achieved apart from frequencies at the edge of the band. Meanwhile, one single sub-band property is plotted to show the robust wideband locking with a locking range of 2.9 GHz.

IV. Fellowship Impact and Career Plan

It is my great honor to receive the recognition of IEEE MTT-S for the 2019 Graduate Fellowship for the year 2019. This award encourages me to further discover the unknown area in mm-wave wideband signal generation. And it allows me to complete my research project for my doctoral studies. I will continue my research career in academia to further develop mm-wave circuit architectures and discover their potential applications. The beauty of the circuits encourages me to push forward my research, and the recognition of this fellowship gives me the power to go further.

References

[1] J. Zhang, et al., "A 21.7-to-41.7-GHz injection-locked LO generation with a narrowband low-frequency input for multiband 5G communications," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 1, pp. 170-183, Jan. 2020.

[2] J. Zhang, et al., "An injection-current-boosting locking-range enhancement technique for ultra-wideband mm-wave injection-locked frequency triplers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3174-3186, Jul. 2019.

[3] J. Zhang, et al., "Analysis and design of ultra-wideband mm-wave injection-locked frequency dividers using transformer-based high-order resonators," *IEEE J. Solid-State Circuits*, vol. 53 no. 8, pp. 2177-2189, Aug. 2018.

[4] J. Zhang, et al., "A 22.4-to-40.6-GHz multi-ratio injection-locked frequency multiplier with 57.7-dBc harmonic rejection," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2020.