Time-Interleaved Switched Capacitor Delays and their Application in Microwave Design

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***Abstract*— Conventional miniaturization techniques of the passive reciprocal/non-reciprocal components offer implementation size advantage at the cost of operational bandwidth. In this work, we introduced an N-path switched-capacitor delay line that overcome the delay-bandwidth-size limit of conventional LTI delay lines, by achieving a delay that is dependent on the clocking scheme rather than its constituent passive component values. Such compact, wide-band, reconfigurable delay network enable a new paradigm of microwave component design by enabling a family of highly miniaturized, non-reciprocal and reconfigurable devices. To this end, we demonstrated an ultra-compact, ultra-wideband circulator, and an FD receiver with FIR-based self-interference cancellation in RF and BB domains, by leveraging compact delays offered by these switched-capacitor delays.**

Index Terms— circulators, delay lines, full-duplex, switched-capacitor, LPTV, ultra-wideband (UWB).

I. Introduction

Passive components such as couplers, circulators and isolators are vital in wireless/optical communications. However, conventional linear, time-invariant passive components built from traditional materials are subject to fundamental limitations associated with reciprocity, size, bandwidth and loss. In order to overcome barriers associated with size and aiming for compact implementations, miniaturized couplers based on lumped components [1] and slow-wave coupled microstrip lines [2] were proposed in the past. However, despite all miniaturization efforts, these microwave devices still occupy a significant area, exhibit compromised bandwidth, and lack reconfigurability.

On the other hand, a traditional way to overcome the limitations of reciprocity is by using ferrite materials which are incompatible with monolithic fabrication process, thus leading to large form factor and implementation costs. In the recent past, there has been a significant interest in implementing magnetic-free non-reciprocal components using time modulation of permittivity [3] and conductivity [4]. However, their bandwidths and frequency tunability have been limited to a fraction of the center frequency and their footprints have been large due to the use of LC resonators or wavelength-scale transmission lines.

In this work, we introduced an N-path (time-interleaved) switched-capacitor delay line that achieves a delay that is set by the clock path, rather than by its constituent passive component values. This allows the reconfiguration of the delay without the reconfiguration of the passive components, also enabling a form-factors which are 100-1000× smaller than the existing alternatives. This N-path delay line concept has been extended to an ultra-wideband (UWB), N-port CMOS circulator with a miniaturization factor of 10^7. We also demonstrated a full-duplex (FD) receiver with wideband FIR-filter-based SI cancellation in RF and BB domains, by leveraging compact delays offered by these switched-capacitor delays.

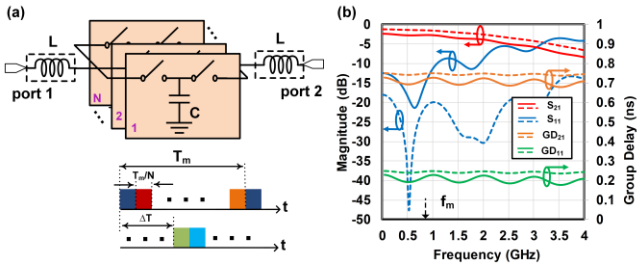

Figure 1. (a) N-path quasi-electrostatic delay. (b) S-parameters of one section with (dotted) and without (normal) the matching inductors when N = 8, f_m=1GHz, ΔT=250ps and L=1.4nH.

II. Breaking the Delay-Bandwidth Product Using Commutated Multipath Networks

Fig. 1(a) shows a 2-port commutated N-path switched-capacitor network where the output switches are delayed with respect to the input set by time $\Delta T > T_s/N$. Such N-path networks have thus far been explored in two asymptotic regimes – filtering, where $RC>>T_s/N$ and sampling, where $RC<<T_s/N$. Here we focus on the rather unexplored regime of $RC\sim T_s/N$ in which case the structure behaves as a low-loss non-reciprocal ultra-broadband delay element [5]. To improve matching to the port impedance Z_0, small inductors can be added on either side of the network (Fig. 1(a)). Simulated s-parameters and the corresponding group velocities of the structure with and without the matching inductors are depicted in Fig. 1(b). The network imparts non-reciprocal temporal delays in the forward and reverse directions ΔT and $T_s - \Delta T$, respectively. Aliasing free bandwidth of this delay element is $Nf_s/2$, while the delay element ideally has <3dB transmission loss from DC to $Nf_s/4$. Hence, by increasing the number of paths N, one can increase the bandwidth of the delay element. Unlike LTI systems, the delay imparted to the signal is largely independent of the component values (L, C, and Z_0) and the frequency of operation, and only depends on the delay between the staggered clocks ΔT and ($T_s - \Delta T$), enabling delay reconfigurability.

III. UWB Quasi-Electrostatic N-Port Circulator

To demonstrate how this new delay element can be used to synthesize wideband microwave components with ultra-compact size, we extended the concept to an N-port commutated N-path network which exhibits extremely wideband N-way non-reciprocity[6]. The proposed N-port

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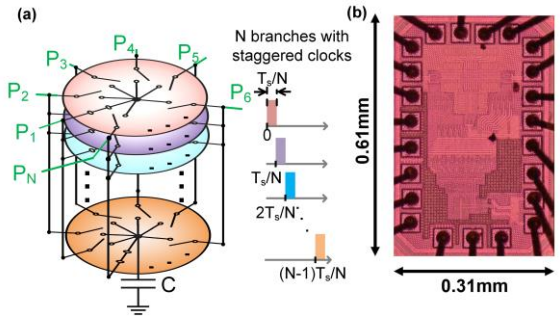

Figure 2. (a) Schematic and timing diagram of the N-Way circulator realized using N-port switched capacitor layers. (b) Chip microphotograph of the 3 port UWB circulator implemented in a 65nm CMOS process.

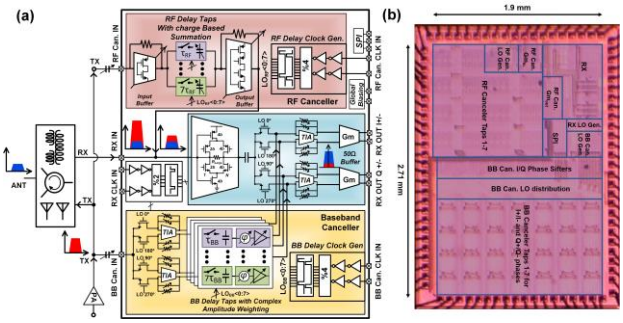

Figure 3. (a) Circuit diagram of the delays taps of the BB canceler and its complex amplitude scaling and summing using a Cartesian phase shifter. (b) Chip micrograph of the FD receiver implemented in a 65nm CMOS process.

circuit consists of N identical layers connected in parallel to N ports as depicted in Fig. 2(a). The switches in each layer are modulated in a revolving fashion so that only one switch in each layer is connected to the capacitor at any time instant. The revolving switching produces direction-dependent transmission (non- reciprocity and N-port circulation), i.e. transmission from port 1 to port 2, from port 2 to port 3, and so on, and isolation in the opposite direction. This architecture overcomes the limitations of prior non-magnetic CMOS circulators that rely on quarter-wave structures, and are consequently limited in their instantaneous bandwidth [3],[4].

As a proof of concept, we implemented a 3-port UWB circulator in 65nm bulk CMOS [7], and Fig. 2(b) depicts the chip microphotograph. The circulator consists of 8 parallel non-overlapping layers, with each consisting of a 2.5pF capacitor connected to 3-ports through three 51µm/60nm transistors. We leveraged the inductance from bond wires as the 3nH inductor required for matching, resulting in an extremely compact area of 0.19mm^2. We measured symmetric performance across the 3 ports for 500MHz modulation and DC – 1GHz operation, with transmission losses ranging from 3.1dB - 4.3dB, isolation > 18dB, matching< -15dB, and noise figure ranging from 3dB – 4dB. This represents the first instantaneously ultra-wideband circulator implemented in CMOS while featuring a footprint that is 100-1000× smaller than prior art.

IV. Full-Duplex Wireless Receiver Featuring RF and BB Cancelers Based on Switched Capacitor Delays

Leveraging these concepts of compact switched capacitor delays, we implemented a full-duplex receiver with integrated RF and baseband (BB) FIR cancelers. The RF and BB cancelers consist of 7 switched-capacitor-based delay taps, each with a delay ranging from 0.2ns-1.1ns and 10ns-75ns respectively, and gain control of 5 bits and 7 bits, respectively (Fig. 3(a)). To reduce the chip area, 7 parallel delay taps are designed with progressive phase shift in their clocking signals as opposed to series cascade of multiple delays with matching inductors. The RF delays taps realize delays of $T_{m,RF}/8$, $2T_{m,RF}/8$, … $7T_{m,RF}/8$. In the RF canceler, the signal summing across the taps and amplitude scaling is achieved in a fully passive way at the output node of the delay units in charge domain. The output of the RF canceler is injected at the input of the LNA to obtain RF SIC (first stage of SIC). Similarly, the BB delay taps realize delays of $T_{m,BB}/8$, $2T_{m,BB}/8$, … $7T_{m,BB}/8$. The outputs of the delay cells are passed on to vector modulator phase shifters, whose outputs are added in current domain and are injected into the RX chain at the outputs of the mixer to obtain the BB SIC.

Fig. 3(d) depicts the chip microphotograph and occupies an area of 5.15mm^2. The taps show delays ranging from 0.2ns-1.1ns in the RF domain and 10ns-75ns in the BB domain when clocked at 1GHz and 11MHz respectively. We measured a cancellation of 13.1dB and 17.1dB from RF and BB cancelers over 20MHz BW at ~700MHz. Owing to the cancellation at the LNTA input by the RF canceler, the TX-induced RX P1dB of the FD receiver with 20dB gain has been enhanced from +2dBm to +9dBm. Under cancellation, the RF and BB cancelers degrades the noise figure of the receiver by 1.1dB and 0.8dB respectively.

V. Career Plan

After my graduation, I would like pursue an academic career in one of the top-tier research universities in the United States. Being granted the IEEE MTT-S graduate fellowship for 2019 has helped me deeply by providing a great boost to my confidence and recognition in the scientific community. I am immensely thankful to IEEE MTT-S society for providing me an opportunity to visit IEEE IMS/RFIC 2019. I look forward to participate in the future events hosted by IEEE MTT-S society.

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