# High-Density Terahertz Imaging System at 2.8 THz in Silicon

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***Abstract*—Terahertz waves are non-ionizing (unlike x-rays), have better spatial resolution than microwaves, and can penetrate optically opaque materials. These qualities make the terahertz region particularly attractive to applications in biomedical imaging, security screening, communications, spectroscopy, and nondestructive evaluation. Recent research has focused on the miniaturization of terahertz technology, working towards developing on-chip terahertz generators and detectors in silicon processes. We aim to push the boundaries of current terahertz research by designing and fabricating a silicon CMOS-based 100-pixel terahertz camera for real time detection of 2.8 THz radiation. This report focuses on the antenna and front-end detector of this chip. To our knowledge, never before has a system capable of video rate imaging, been designed in standard silicon processes to operate at frequencies above 1 THz.**

***Index Terms*—Terahertz, Terahertz Imaging, CMOS.**

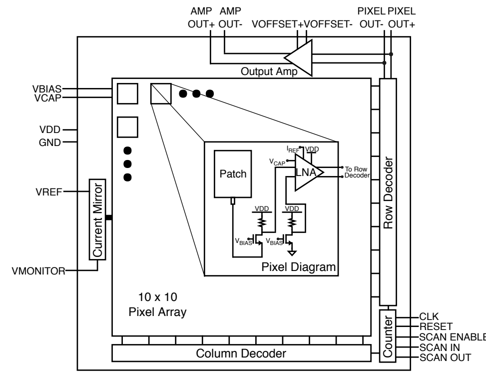


Fig. 1. High level schematic of the full camera chip, showing the 10x10 pixel array, digital readout circuitry, and final output amplifier. The inset shows an overview of an individual pixel.

## I. Introduction

THE only part of the electromagnetic spectrum that remains largely unutilized is that of the terahertz gap, typically defined as the frequency band of 0.3-3 THz [1]. Terahertz waves have several unique qualities that make them attractive for use in applications ranging from biomedical imaging to explosives detection to ultrafast communications. First, terahertz waves are non-ionizing [2], meaning they lack the risk posed to humans by x-rays. Second, terahertz waves have better spatial resolution than microwaves [2]. Third, terahertz radiation is able to penetrate most optically opaque materials [2]. Current technology offers only large, bulky, and expensive terahertz imaging devices. Our research in the design and development of a single-chip silicon-based terahertz camera is motivated by the lack of small, inexpensive devices appropriate for detecting terahertz radiation. Here, we discuss the design of a single-chip 100-pixel 2.8 THz camera focusing on the camera's antenna and front-end detector. This work is described further in [3], while the chip's amplification and digital readout circuitry are detailed in [4] and [5] respectively. The chip was recently fabricated and is currently being tested and characterized.

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## II. Background

Detection of incident radiation that is much higher than the $f_{max}$ of silicon technology (frequency of unity power gain, approximately 300 GHz), is possible based on plasma wave theory and the principle of distributed resistive self-mixing. Plasma wave theory shows that a FET with terahertz radiation coupled between its gate and source has a constant drain-source voltage with a resonant dependency on the frequency of the incoming radiation [6]. This theory was combined with classical resistive self-mixing into the distributed resistive self-mixing, which says that terahertz radiation incident on the gate of a FET generates a time-varying channel current and resistance that result in a DC drain-source voltage proportional to the incident power [7].

Using these principles, each pixel couples radiation incident on a patch antenna to a common gate detector. A low-noise amplifier compares the antenna-coupled voltage with a reference voltage, amplifies it and sends it to digital readout circuitry. The overview of our chip is shown in Fig. 1, with the pixel design detailed in the inset.

## III. Antenna and Detector Design

Patch antennas are a popular antenna geometry for on-chip terahertz detectors because of their broadside radiation pattern and planar profile, which facilitates integration within a standard CMOS process. Each pixel in our design consists of a patch measuring 20 $\mu$m x 30 $\mu$m, that is fabricated in the two uppermost metal layers of the CMOS process. There is a ground plane contact located at the center of the patch as seen in Fig. 2. This via provides a path for the transistor's DC current to flow to ground. By locating it in the center of

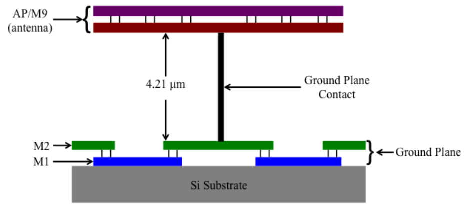


Fig. 2. Cross section of the antenna as integrated on-chip. The ground plane contact is necessary to provide a path for DC current through the detector.

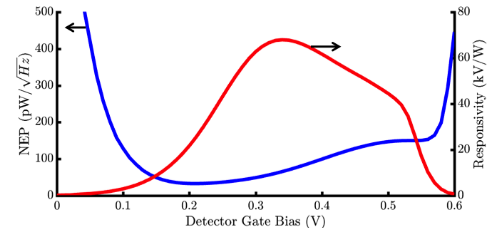


Fig. 3. Simulated responsivity and NEP of the full pixel, accounting for parasitic resistances and capacitances due to the layout.

the patch, where the field intensity is zero, it causes minimal disruption to the radiation pattern.

A minimum-sized common gate detector, shown in the inset of Fig. 1, was used for this design. It consists of one transistor coupled at its source to the patch antenna and a second transistor with a grounded source that is used as a reference. Based on the principle of distributed resistive self-mixing, a change in DC voltage ($\Delta V_{DC} = V_{ANT} - V_{REF}$) is observed between the drains of the two transistors when the antenna is subjected to terahertz radiation. The function of the reference detector is analogous to unexposed (dark) pixels in a standard consumer CMOS camera that reduce noise by providing information about dark current levels.

## IV. Simulated Performance

The performance of a detector system is described by its responsivity ($R$) and noise equivalent power (NEP). Responsivity is a measure of detector gain relative to the incident power, $R = \Delta V_{DC}/P_{IN}$, expressed in V/W. NEP is the noise equivalent input power, defined as the input signal power that results in a unity signal-to-noise ratio (SNR) over a 1 Hz bandwidth at the detector output, measured in units of W/$\sqrt{\text{Hz}}$. NEP quantifies the detectors sensitivity and is calculated as $\text{NEP} = \sqrt{\overline{v_{no}^2}}/R$, where $\overline{v_{no}^2}$ is the output noise power spectral density integrated over the bandwidth of interest (bandwidth of the following stage for a video rate imager). This value is typically normalized to a 1 Hz bandwidth for comparing detectors of different bandwidths or imaging modes [8].

The responsivity and NEP of a simulated pixel are shown in Fig. 3. These results include the operation of the antenna, detector and low-noise amplifier and are simulated in Cadence, using an extracted components to account for layout-specific parasitic resistances and capacitances. Because Cadence extraction does not capture parasitic inductances or the radiating effects of the antenna, these are characterized by HFSS simulations and then combined with the Cadence results. The simulated maximum responsivity of each pixel is 67.9 kV/W, which occurs for a detector gate bias of 340 mV. The simulated minimum NEP is 32.9 pW/$\sqrt{\text{Hz}}$, which occurs for a detector gate bias of 210 mV. As seen in Fig. 3, there is a tradeoff between gain and sensitivity so the bias voltage of the detector must be chosen appropriately according to a specific application's needs.

## V. Conclusions and Future Work

This camera chip extends the boundaries of existing terahertz imagers in two main ways. First, it detects incident radiation at 2.8 THz, whereas existing silicon-based terahertz imagers only operate below 1 THz. Second, it supports video rate imaging, which is essential for real time camera operation and provides additional benefits in many applications. The major accomplishment of this project was successful tapeout of the chip in the TSMC 65 nm process.

The chip was fabricated and is currently undergoing testing and characterization. If the chip functions as designed, this research will potentially enable groundbreaking, low-cost, portable solutions in biomedical sensing, security screening, nondestructive evaluation, ultra-fast wireless communications, and spectroscopy.

## VI. MTT-S Scholarship Impact

After graduating in June 2018 from Princeton University, I began the Ph.D. program in Electrical Engineering at Stanford University. I am excited to continue research in developing advanced sensor systems while at Stanford. I would like to express my gratitude to IEEE MTT-S for supporting of this research, as well as my attendance at the 2018 Latin America Microwave Conference. Attending LAMC and presenting this research there was a great experience. I appreciated the chance to network and see how IEEE and MTT-S are committed to supporting technical research outside of the United States.

## References

[1] T. H. Lee, "Terahertz CMOS integrated circuits," in *2014 IEEE Int. Symp. Radio-Frequency Integr. Technol.* IEEE, Aug 2014, pp. 1–2.

[2] M. Tonouchi, "Cutting-edge terahertz technology," *Nat. Photonics*, vol. 1, no. 2, pp. 97–105, 2007.

[3] A. Broome, "Single-Chip 100-Pixel 2.8 THz CMOS Camera: Antenna and Front-End Detector Design," B.S.E. thesis, Princeton University, Princeton, NJ, May 2018.

[4] T. Smith, "100-Pixel 2.8 THz CMOS Camera: Analog Circuitry Design," B.S.E. thesis, Princeton University, Princeton, NJ, May 2018.

[5] D. Stanley, "Single chip 100 pixel CMOS THz Camera at 2.8 THz," B.S.E. thesis, Princeton University, Princeton, NJ, May 2018.

[6] M. Dyakonov and M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 380–387, Mar 1996.

[7] A. Lisauskas, U. Pfeiffer, E. Öjefors, P. Haring Bolìvar, D. Glaab, and H. G. Roskos, "Rational design of high-responsivity detectors of terahertz radiation based on distributed self-mixing in silicon field-effect transistors," *J. Appl. Phys.*, vol. 105, 2009.

[8] V. Mackowiak, J. Peupelmann, Y. Ma, and A. Gorges, "NEP-noise equivalent power," Thorlabs, Inc., Newton, NJ, Tech. Rep.