A 325 GHz InP HBT Differential-Mode Amplifier

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***Abstract*—An MMIC amplifier operating at the highest reported frequency up to date for indium-phosphide double-heterojunction bipolar (DHBT) transistor technology is presented. The amplifier chain consists of seven unit-cell stages that contain differential-pair common-base HBTs and compact inverted microstrip matching networks. Amplifier operation in differential mode generates a virtual RF ground at a convenient location inside the unit cell. The measurements at 325 GHz show a small signal gain of 25 dB and a maximum output power of −1.5 dBm. An amplifier gain of greater than 20 dB is observed over 60 GHz bandwidth extending from 285 to 345 GHz.**

***Index Terms*—InP HBT, monolithic microwave integrated circuit (MMIC), terahertz amplifier.**

I. Introduction

TERAHERTZ front-end transceivers built from electronic ICs are the key components of small-aperture high-resolution imaging arrays and high data-rate communication systems. High-frequency InP transistors for both HEMT and HBT types with their cutoff frequencies reaching well into the terahertz range are now available, and integrated amplifier and oscillator circuits operating above 300 GHz have been demonstrated with supports from DARPA projects such as submillimeter wave imaging focal-plane-array technology (SWIFT) [1]. HEMT-based waveguide-module amplifiers have recently demonstrated better than 10 dB of gain at 0.48 THz [2] and 10 mW of output power at 338 GHz [3]. Comparable progresses are being reported on HBT amplifiers as in the case of a differential-mode amplifier exhibiting 17 dB of gain at 290 GHz [4]. This letter describes modifications made on the previous HBT amplifier design to achieve a considerable amount of improvements on the gain and bandwidth. In addition, the results of power measurement performed for the first time on HBT amplifiers at a frequency above 300 GHz are included.

II. Device Technology

The HBT structure is grown using molecular beam epitaxy and contains a 30 nm carbon-doped base layer and a 150 nm N-InP collector region. The emitter contact is patterned using electron-beam lithography and formed using an Au-based electroplating process. A thin emitter semiconductor stack of less than 100 nm minimizes undercut during the self-aligned emitter mesa etch. After dielectric sidewall spacers are added to passivate the base-emitter junction and permit the formation of a self-aligned base contact, the remaining process flow follows that of a standard mesa-HBT process [5]. The device layer is passivated with an 0.8 μm benzocyclobutene (BCB) layer before planarization etch is applied to expose the emitter post. The impedance matching network is built using three interconnect metal layers as shown in Fig. 1. In consideration of radiation loss and device location, inverted microstrip lines formed with 1 μm thick M1 and M2 metals as the signal line and the ground plane are primarily used in the design. The fabrication technology also includes thin-film resistors (50 Ω/sq) on the device layer and MIM capacitors on the M1 layer. The devices that are selected for the amplifier design have an emitter area of $0.25 \times 6\mu\text{m}^2$. When biased at a collector current density of 1 $\text{mA}/\mu\text{m}^2$, these devices show a dc beta of nearly 30 with an estimated f_{T} of 350 GHz and $f_{\max}$ of 750 GHz.

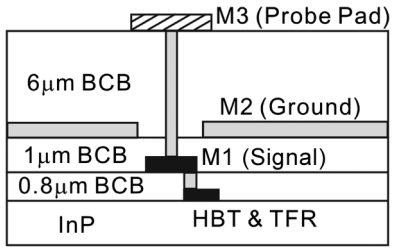

Fig. 1. Three interconnect metal layers used in the amplifier design.

III. Amplifier Design

In order to obtain better than 20 dB of gain above 300 GHz, seven identical unit-cell stages are connected in cascade to compensate for the low available gain from a single device. RF-ground connections normally require bulky bypass capacitors and M1-to-M2 vias resulting in extra phase delay and lower gain. These ground connections can be removed with the use of a virtual ground that is generated when the amplifier is driven in differential mode. Input and output baluns best suited to the interconnect-layer profile are designed for single-to-differential mode conversion over a broad frequency band.

A. Unit Cell

The unit cell, with its schematic shown in Fig. 2(a), contains common-base differential-pair HBT devices. Initially, the HBTs in common-base configuration sustain more than 10 dB of available gain at 300 GHz unaffected by the base-to-collector para-

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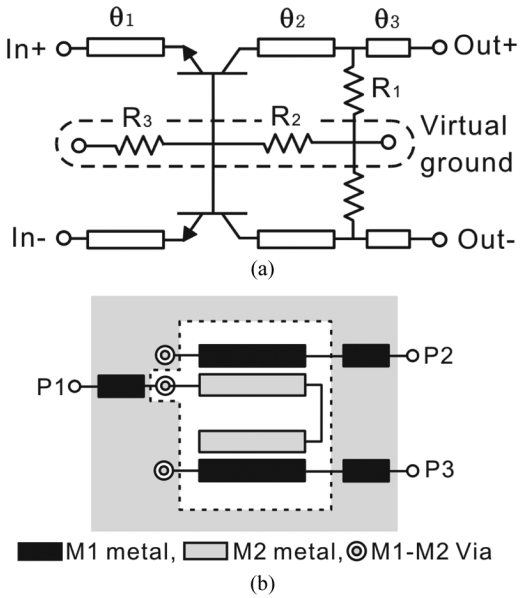

Fig. 2. Circuit schematics for the two main components in the amplifier design, (a) the unit cell and (b) the Marchant balun.

sitic capacitance. However, the available gain is lowered to 4 dB when a stabilizing shunt resistor of 90 Ω is added to the collector terminal. The main advantage of the CB configuration is in the implementation of a current-reuse dc-bias network where all the cascaded devices are biased in series using a single external power supply. The unit-cell matching network contains three short inverted microstrip sections with 300 GHz electrical lengths θ_1, θ_2, and θ_3 of 17°, 5°, and 4°, respectively. Short-circuited shunt stubs normally employed in dc-bias networks are purposely avoided to prevent narrow gain bandwidth. The width of all the microstrip sections is fixed at 2 μm to maintain 50 Ω characteristic impedance. Electromagnetic (EM) simulations at 300 GHz indicate a small radiation loss of 0.4 dB, but a significant conductor loss of 2.4 dB for a 520 μm line representing one wavelength when metal conductivity of 4×10^7 S/m is assumed. The dc-bias network consisting of four resistors for each unit cell establishes a collector-to-emitter voltage of 1.35 V and a collector current of 10 mA with the resistances R_1, R_2, and R_3 of 90, 90, and 200 Ω, respectively. In addition to offering more compact unit-cell design, the differential-mode virtual ground prevents resistors *R2* and *R3* from interfering with the RF gain while the collector shunt resistor *R1* improves stability at the expense of reduced gain and output power. The area of the unit-cell layout is 30 μm wide and 40 μm long.

B. Marchant Balun

The three-port balun structure, as described in Fig. 2(b), essentially consists of two quarter-wave coupled-line sections. A broadband impedance matching at port 1 requires a large even-mode impedance of greater than 100 Ω obtainable with a rectangular opening in the M2 ground. An odd-mode impedance of 25 Ω is also necessary for an equal amount of power transfer to ports 2 and 3. A coupled-line structure using both M1 and M2 metals for broadside coupling is proposed to facilitate an accurate odd-mode impedance tuning. Slight adjustments are made

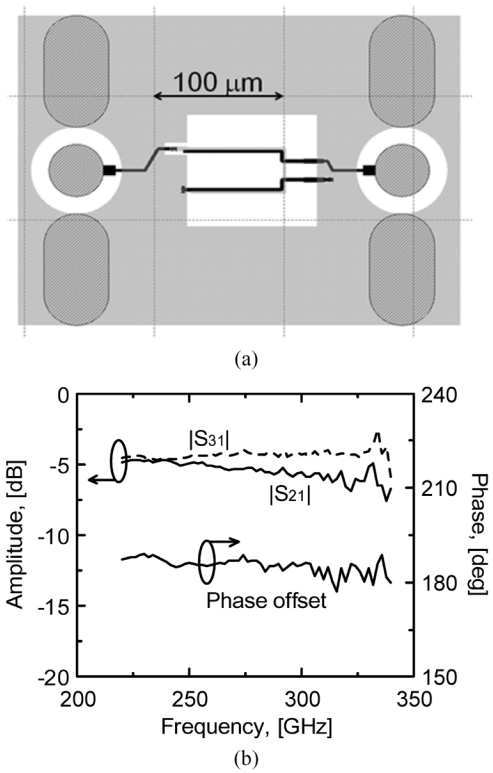

Fig. 3. (a) Marchant balun layout and (b) the measured results.

to the lengths of the coupled-line sections and the extra connecting lines to maintain a proper center frequency.

C. Complete Amplifier

The Marchant baluns and the unit-cell chain are combined to complete the amplifier design. Extra matching networks using shunt stubs are inserted between the baluns and the unit-cell chain for 50 Ω matching. RF probe pads using M3 metal are added to the edge to complete the amplifier design. The dc bias is applied through the output balun and the collector terminals of the last-stage devices. The area of the final amplifier layout is 680×340 μm^2.

IV. Measurement Results

Amplifier S-parameters are measured using two types of network analyzer frequency-extension modules for 220–325 GHz (WR-3) and for 325–500 GHz (WR-2.2) bands. An inverted microstrip line, 2 μm wide and 150 μm long, shows an average insertion loss of 1.0 dB and an impedance matching of better than 10 dB near 300 GHz. Measurements on two separate circuits both containing a single balun with 50 Ω termination on the unprobed port as shown in Fig. 3(a) provide a full three-port data. The results in Fig. 3(b) show a phase offset close to 180° and an extra insertion loss of 2 dB over WR-3 band. Although the amplitude imbalance increases to 2 dB above 300 GHz, its impact on the amplifier gain is expected to be negligible. The S-parameter datasets for the two frequency bands are taken from the amplifier shown in Fig. 4(a) with the same dc bias of 9.5 V and 20 mA. At the boundary frequency of 325 GHz, the two

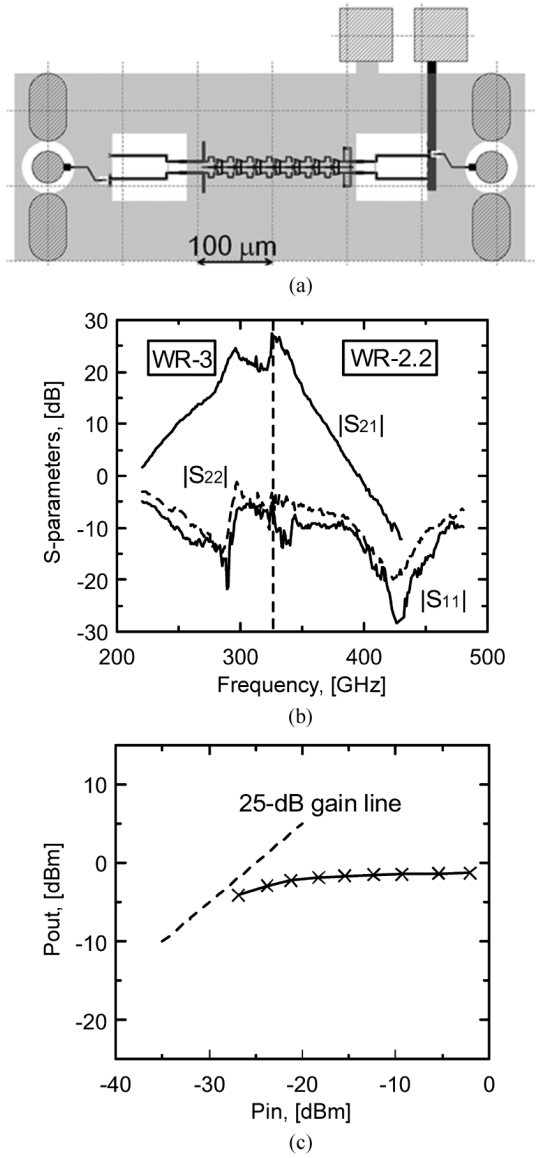

Fig. 4. (a) Amplifier layout, (b) the small signal, and (b) the power measurement results.

datasets show different gain values of 22.8 and 27.3 dB, indicating at least 4.5 dB of measurement uncertainty. Amplifier gain of greater than 20 dB is obtained over 60 GHz ranging from 285 to 345 GHz as shown in Fig. 4(b). In addition, the gain curve responds accordingly to the dc bias, confirming a stable amplifier operation. The input and output return losses stay below 0 dB, showing similar frequency responses due to the losses present in the input and output baluns. The amplifier power measurement is carried out at 325 GHz with a multiplier chain from Virginia Diode, Inc., and an Erickson Instruments LLC PM4 power meter. A simple calibration process using an on-wafer microstrip delay line provides the path-loss estimation for the measurement system. The results plotted in Fig. 4(c) together with 25 dB gain reference line show that the maximum output power approaches -1.5 dBm while the 1 dB saturation power is estimated to be about -5 dBm. Although the device model is not fully developed at the moment, the simulations predict the maximum output power of 4 dBm with a broader small-signal gain bandwidth.

V. Conclusion

A seven-stage differential-mode amplifier using state-of-art InP DHBT devices produces more than 20 dB of small-signal gain over 60 GHz bandwidth centered at 315 GHz. The amplifier containing two $0.25 \times 6 - \mu\text{m}^2$ HBTs in its last stage that is biased at 1.35 V and 20 mA produces the maximum output power of -1.5 dBm at 325 GHz.

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