32 dBm Power Amplifier on 45 nm SOI CMOS

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***Abstract*—A silicon metal-semiconductor-field-effect-transistor (MESFET) power amplifier operating at 900 MHz fabricated on a 45 nm silicon-on-insulator CMOS process with no changes to the process flow is presented. The soft breakdown of the MESFET is 20 times that of the MOSFET and allowed a single transistor amplifier based on Class A bias conditions to operate at up to 32 dBm output power with an 8 V drain bias. The amplifier had a peak power added efficiency of 37.6%, gain of 11.1 dB, OIP3 of 39.3 dBm and 1 dB compression point at an output power of 31.6 dBm. The device required only 0.125 mm^2 of active area. Additionally, the depletion mode operation of the MESFET enables a simple input bias approach using an inductor to ground at the gate of the device.**

***Index Terms*—Metal-semiconductor-field-effect-transistor (MESFET), power amplifiers (PAs), silicon-on-insulator (SOI) technology.**

I. Introduction

THE demand for wireless technologies on a global scale continues to grow and is one of the leading markets for the semiconductor industry. Of paramount consideration is the overall cost of the device which is one of the main drivers for using silicon CMOS for as much of the handset as possible. However, a large barrier to complete silicon integration is the power amplifier (PA), especially on scaled technologies with low operating voltages that are ideally suited for the digital circuitry. At low voltages more current is required to meet output power specifications resulting in low impedances that are difficult to attain at the PA output.

One common solution is to develop a module which contains several die from different technologies bonded to a laminate; often including GaAs HBT PAs, a pHEMT RF switch and a HVCMOS power management die [1]. This requires the use of several high cost technologies and current research is focused on developing CMOS only approaches that achieve Watt level output powers [2]–[4]. Alternative CMOS based technologies with higher breakdown voltages have been presented including a modified CMOS process [3] and a modified LDMOS process [1] but both require more complicated transistor structures; specifically in the gate region of the device. Another method is to stack multiple CMOS devices so the drain voltage is distributed but careful attention must be paid to the gate bias of each device which can complicate the design [4].

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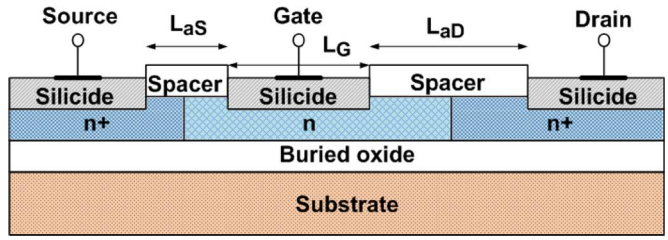

Fig. 1. Cross-sectional view of the enhanced voltage MESFET device fabricated on the 45 nm technology with no changes to the CMOS process flow.

In this letter, we present a silicon MESFET based PA operating at up to 32 dBm output power fabricated on a 45 nm SOI CMOS process with no changes to the process flow. The major benefit of the MESFET is that it can operate at up to 20 times the breakdown voltage of the CMOS and a single transistor design can be employed thus simplifying the PA circuitry. This letter demonstrates the first SOI MESFET PA operating at over a Watt of output power. To our knowledge, the MESFET enables the highest breakdown voltage and output power demonstrated for a single, non cascoded device to date in a 45 nm technology.

II. Silicon MESFET Device

The MESFET is fabricated by aligning a metal silicide Schottky gate over a lightly doped *n*-well and a cross section is shown in Fig. 1. A detailed fabrication process flow has been presented in [5]. Spacer layers used to separate the gate from the drain and source regions are a key step in the process flow and can be used to tune the breakdown voltage (V_{BD}) and f_T of the device. The minimum dimensions of the source and drain access regions formed by the spacer layers, L_{aS} and L_{aD} and the Schottky gate length L_g are process dependant and usually one to five times larger than the critical dimensions of the technology node.

The general silicon MESFET dc and RF characteristics have been measured and Table I shows a comparison between devices with 500, 1000, and 2000 nm drain and access regions which have V_{BD} of 15, 21, and 28 V, respectively. The MESFETs are depletion mode devices and have threshold voltages of approximately -0.5 V with low gate leakage currents [6].

III. Amplifier Design and Experimental Results

For the high breakdown, high f_T MESFET used in the PA presented here, L_g was 200 nm, $L_{aS} = L_{aD} = 1000$ nm, and the gate width, L_W, was 30 mm. The device was chosen as a compromise between $\mathrm{V_{BD}}$ and f_T (Table I). The total active die area was only 0.125 mm^2. The MESFET family of curves (FOC) for a device with the same geometry and LW of 0.3 mm is shown in Fig. 2 and demonstrates good characteristics to greater

TABLE I
MESFET CHARACTERIZATION SUMMARY

Parameter	L_{aS} and L_{aD} = 500nm	L_{aS} and L_{aD} = 1000nm	L_{aS} and L_{aD} = 2000nm
Gate oxide	*No Gate Oxide*	*No Gate Oxide*	*No Gate Oxide*
L_g (nm)	200	200	200
L_{aS}/L_{aD} (nm)	500	1000	2000
W_{finger} (μm)	15	15	15
V_{BD} (V)	15	21	28
f_T (GHz)	24	17.5	9
f_{MAX} (GHz)	35	25	20
V_T (V)	-0.5	-0.5	-0.5

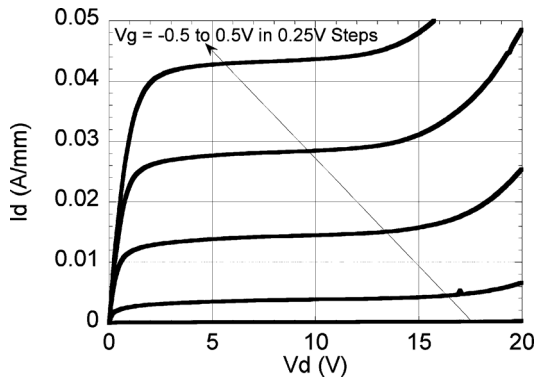

Fig. 2. The measured family of curves for a MESFET with $L_g = 200$ nm and $L_{aS} = L_{aD} = 1000$ nm that was used for the RF PA.

than 15 V. In contrast, the recommended operating voltage of the standard CMOS devices in this 45 nm technology is less than 1 V.

The MESFET is a depletion mode device and when in the saturation region, a gate voltage of 0 V is sufficient to place the dc bias near a Class A loadline bias point of $I_{\mathrm{MAX}}/2$. Therefore, the input network can be greatly simplified by directly connecting an inductor to the ground plane at the gate. Fig. 3(a) shows the schematic of the amplifier circuit with an L-match network at the output which was realized with microstrip line and a capacitor to ground. In order to determine the load conditions for the L-match, a simple Class A loadline approach was used where $R_{\mathrm{load}} = V_{\mathrm{DC}}/I_{\mathrm{DC}}$ [7]. Based on the FOC in Fig. 2, the 30 mm device biased at $V_g = 0$ V, $V_{\mathrm{DC}} = 8$ V predicts $I_{\mathrm{DC}} = 450$ mA, $R_{\mathrm{load}} = 18\ \Omega$ and an output power of 32.5 dBm. These conditions were used for the final amplifier design on an FR4 PCB board. A lambda/4 line was used for the drain bias and it was terminated with a capacitor to ground with self resonant frequency near the frequency of operation, 900 MHz.

After initial power measurements de-embedded to SMA connectors, it was found that adding a capacitance of 4.7 pF to the gate line improved the input match and increased the output power. Fig. 3 shows the final board design attached to a solid copper block to improve thermal properties. The MESFET transistor was mounted to a Kyocera A191 package and bonded with four source, two drain and two gate wires.

The PA was measured at 900 MHz with a drain bias of 8 V and the recorded output power and efficiency are shown in Fig. 4. The amplifier had a peak power gain of 11.1 dB, drain

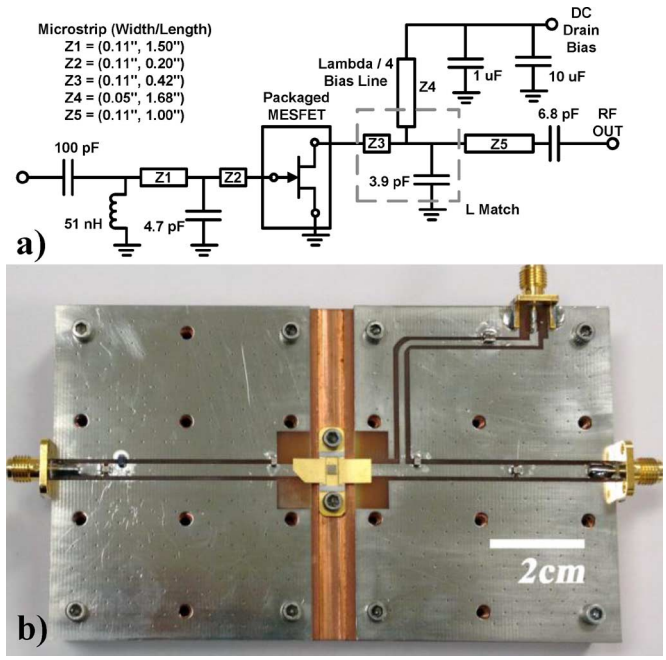

Fig. 3. (a) Circuit schematic of the final PA using a single MESFET transistor and inductor to ground for gate biasing. (b) Photograph of the board level design for the 900 MHz MESFET.

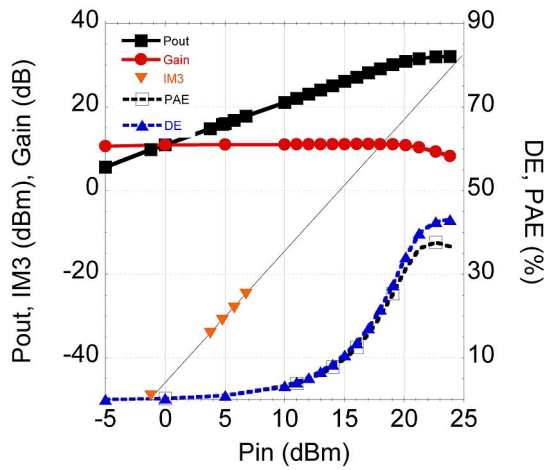

Fig. 4. Measured output power, gain, DE, PAE and IM3 at 1 MHz tone spacing for the PA at a drain bias of 8 V operating at 900 MHz. Symbols represent measured points and the solid line for IM3 is an extrapolation.

efficiency (DE) of 43% and power added efficiency (PAE) of 37.6%. For this PA, the focus was not on maximizing PAE and future work will include higher efficiency amplifiers such as Class E. The 1 dB compression point of 31.6 dBm was at an input power of 21.6 dBm for this bias condition. Two tone, third order intermodulation measurements (IM3) where performed at 900 MHz and 1 MHz spacing (Fig. 4, symbols) and the OIP3 was extrapolated to be 39.3 dBm. The silicon MESFET PA was then measured at different drain biases and output power, gain and PAE at the 1 dB compression point are shown in Fig. 5. At a backed off voltage of 3.3 V, the amplifier shows almost the same gain but a reduction in output power to 24.5 dBm and PAE to 22.7% because the load L-match network is no longer optimized.

The 3 dB bandwidth of the PA at an input power of 20 dBm was measured from 100 MHz to 1050 MHz and is shown in

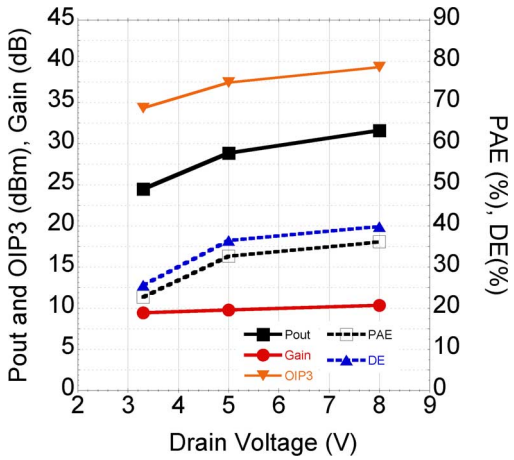

Fig. 5. Measured output power, gain, DE, PAE at the 1 dB compression point and extracted OIP3 at different drain biases operating at 900 MHz. Symbols represent measured points.

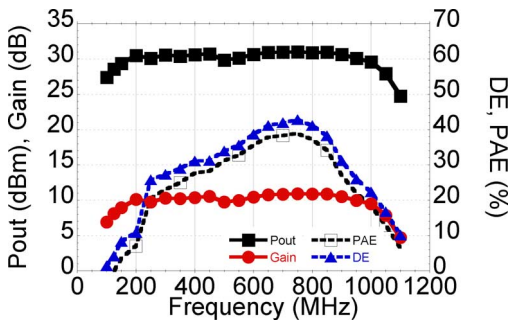

Fig. 6. Measured output power, gain, DE, PAE of the amplifier biased at 8 V across different frequencies. Symbols represent measured points.

Fig. 6. The amplifier has a wide bandwidth because of the nature of the matching networks at the gate and drain. At the gate side, the single 51 nH inductor used as the bias provides an impedance of Ls which is a dc short to ground and attenuates frequencies beyond that of the PA range of operation. The drain side L-match is wideband because the transformation ratio of the 18 Ω impedance presented to the transistor and 50 Ω output impedance is only 2.8.

The MESFET PA is relatively robust because the device has a Schottky junction gate instead of a fragile gate oxide. Currently, the device has been fabricated and measured with no electrostatic discharge protection on the die. This simplifies the PA and other designs because additional parasitics are not present. Moreover, the MESFET structure on this 45 nm process has been tested for extreme environment applications and shows little degradation during stress testing. When biased at a drain voltage of 10 V and held at a temperature of 160°C for 168 h, there was little shift in the family of curves and gate currents [8]. Statistical measurements of the threshold voltage and drive current indicate that the device has low variation and high yield [8].

IV. Conclusion

In this letter, the first Watt level PA using silicon MESFETs fabricated on a scaled 45 nm SOI CMOS technology is reported. We are currently investigating modeling the MESFET for PA applications with a focus on both a TOM3 and Angelov model fit to nonlinear operation. The high breakdown voltage of the device enables simplified PA designs because the required load resistance transformation ratio is low. Because the device is fabricated in a conventional foundry, it is possible to easily integrate CMOS based control electronics alongside the PA allowing for smaller form factor wireless applications and reduced cost.

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