Continuous Mode Power Amplifier Design Using Harmonic Clipping Contours: Theory and Practice

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Abstract—A novel graphical power amplifier (PA) design tool, the "clipping contour," is introduced and described. Using the now well-publicized continuous Class-B/J voltage waveform formulation as a starting point, a process is derived that allows contours to be constructed on a Smith chart that define the "zero-grazing" fundamental and harmonic impedance conditions. Theoretical equations are defined and solved whereby the contours can be drawn in real time in a computer-added design environment. A key and novel result from this theory is the definition of a 2-D harmonic design space that opens up rapidly as small concessions from optimum power and efficiency matching conditions are made. A design example is described and fabricated, which demonstrates the utility of using the second harmonic clipping contour during the PA design process. A 10-W GaN demonstrator gives measured continuous wave power >8.5 W, efficiency >60%, and better than -30-dB adjacent channel power ratio over a bandwidth of 1-2.9 GHz.

Index Terms—Class B/J, clipping contour, continuous modes, power amplifier (PA), waveform engineering.

I. INTRODUCTION

P OWER AMPLIFIERS (PAs) are crucial components in almost all communications systems. They typically draw the largest proportion of dc current of all components in the RF transmit chain. As a result, their performance requirements dictate many other factors in the system, such as dc supply voltages, current ratings, cooling requirements, and space. Achieving high efficiency (η) in the PA has thus long been the subject of intense research [1]–[12].

In addition to efficiency, it must be recognized that as the final active component in the transmit chain, the linearity of the PA will make the biggest contribution to the system linearity figures of merit. Modern communication systems place stringent requirements on transmitter linearity by specifying tight error vector magnitude (EVM) and adjacent channel power ratio (ACPR)/alternate channel power (ALT) requirements on the system [13]–[15]. These regulations prevent operation of the PA at high levels of compression; but simply reducing the drive power generally results in lower PA efficiency, thus requiring more or larger PAs to achieve the same transmit

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at http://ieeexplore.ieee.org. Digital Object Identifier 10.1109/TMTT.2013.2292675 power, resulting in an increase in both system purchase and running costs [16].

Numerous techniques have been available, for many years, that are able to improve the "power-back-off" (PBO) efficiency, for example, the Doherty PA [17]–[19]. However, in practice these techniques do not, in general, bypass the need to implement corrective linearization techniques, such as digital pre-distortion, to meet linearity requirements. Implementation of these techniques usually, indeed inevitably, results in further degrade system efficiency.

Some of the distorting properties of the PA are intrinsic, such as non-linearity of the transconductance, and voltage dependence of the various parasitic capacitances. These kinds of nonlinearity, widely characterized in the literature as "weak" nonlinearities, can usually be negated effectively using a predistorter. Clipping effects, however, are "strong" non-linearities and avoiding them requires a waveform engineering approach [20]. By choosing modes in which the transistor is maintained in a quasi-linear region of the I-V characteristic, strong non-linearities can be minimized. The continuum of modes often called Class J or Class B/J (discussed in Sections II and III) and the more recent continuous Class F or Class F/J [21]-[23] are examples of this approach. These modes target clearly defined voltage and current waveforms at the intrinsic current generator of the transistor. The voltage and current waveforms are prescribed to be efficient, but avoid strong interaction with the transistor knee region. Prior work has demonstrated that PAs designed targeting these modes are capable of excellent efficiency, linearity, and bandwidth [22], [24]–[26].

We note here in passing that so-called switch modes, such as Class E [4], do make deliberate use of the knee region in order to implement switching action. As such, knee interaction is not necessarily harmful from an efficiency standpoint alone; here we are primarily concerned with maximizing efficiency while maintaining linearity and predistorter efficacy.

This paper presents again an important extension to the voltage formulation first presented in [21] that empowers the designer to recognize the design tradeoffs when attempting to realize these PA modes. This new formulation defines a larger and more comprehensive set of zero-grazing voltage waveforms that allow for design tradeoffs against the optimum conditions for power and/or efficiency. The result of this is, for any given fundamental impedance (Z_{1F0}), the designer can compute and display a 2-D zone of second harmonic impedance terminations (Z_{2F0}) that will generate a non-clipping voltage waveform. The equations for optimal generation of these second harmonic impedances are derived and discussed in Section IV.

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These impedances can be plotted on a Smith chart; inside the boundary, the generated voltage waveform will stay above zero; outside, the voltage waveform will induce a strong reaction with the knee region, causing the device to clip the current waveform, resulting in poor linearity and ineffective predistortion.

A pair of amplifiers are designed, built, and measured comparing the effect of obeying and violating the boundary area (Section VI). Simulated and measured data is displayed showing the benefits of following the clipping contours condition.

II. CASE FOR CONTINUOUS MODES

The method for defining the waveforms of certain specific classical high-efficiency modes of operation, such as Class B, Class D, and Class F, has been well established by Snider, Raab and others [2], [27], [28].

If we define the in-phase and quadrature components of the intrinsic device-plane voltage and current as coefficients of a time-varying trigonometric polynomial, where n is the harmonic order,

$$V(\theta) = V_{\rm DC} + \sum_{n=1}^{N} V_{nr} \cos(n\theta) + V_{nq} \sin(n\theta)$$
$$I(\theta) = I_{\rm DC} + \sum_{n=1}^{N} I_{nr} \cos(n\theta) + I_{nq} \sin(n\theta), \qquad \theta = \omega t.$$
(1)

It is useful to normalize the coefficients to the dc term and define η in terms of the fundamental real voltage and current

$$v_{nr} = \frac{V_{nr}}{V_{\rm DC}} \quad i_{nr} = \frac{I_{nr}}{I_{\rm DC}}$$
$$v_{nq} = \frac{V_{nq}}{V_{\rm DC}} \quad i_{nq} = \frac{I_{nq}}{I_{\rm DC}} \tag{2}$$

thus giving the output efficiency

$$\eta = \frac{v_{1r} * i_{1r}}{2}.$$
 (3)

The formulation assumes a fixed optimal current waveform, chosen for its high i_{1r} to maximize η , that is "universal" for all device sizes and frequencies [29]. A frequent choice is a half-wave rectified sinusoid that can be implemented without the need for complicated drive circuitry. A voltage waveform is selected with a similarly high v_{1r} such that the combination of voltage and current waveforms maximizes the fundamental to dc real power ratio, and thus η .

The voltage waveform must, however, have constraints placed upon it to yield a practically useful result. Firstly, the harmonic content must be suitably low so as to limit the number of harmonics that must be controlled by the matching network; it can usually be assumed that extremely high-order harmonics will generally see impedances close to a short circuit due to the devices parasitic drain–source capacitance.

Secondly, the waveform must comply with the device physics (see Fig. 1). It cannot, at any point in the cycle, attempt to reach a negative value, as this would be resisted by an increasingly strong interaction with the transistor knee/ohmic region, clipping the current waveform, generating considerable non-lineari-



Fig. 1. Waveform boundaries. A STATZ FET model from the AWR Design Environment is used here. Class A dynamic load line overlain upon the DCIV traces to show typical device operation.

ties. If the clipping is extremely strong, this will eventually limit η . An important feature of the clipping contour design methodology is to ensure such non-linear excursions of voltage into the knee region are prevented. In addition, the voltage peaks cannot cause the device to breakdown, i.e., it must have an acceptably low peak value.

All this is performed assuming an ideal device acting as a current generator. Parasitics are ignored and an attempt is made to de-embed these parasitics on a real device to look at the intrinsic or current generator (Igen) impedances.

When translated to the impedance domain, these waveforms result in a single set of matching impedances. The PA designer is then tasked with designing a matching network that fulfills these harmonic impedance criteria. This stipulation is a key frustration for the PA designer, who is provided with matching elements, the impedances of which change significantly over frequency. This inevitably restricts the operating bandwidth of these high-efficiency modes.

One approach to solving this problem is to use filters with a large number of poles to increase the bandwidth. In practice, this is rarely feasible as each additional pole increases the matching circuit loss, resulting in a reduction in both power and η . Continuous modes address this problem by modifying the voltage waveform, changing the harmonic components to incorporate the movement of the circuit impedances in the ideal matching impedance domain. The Class B/J voltage waveform equation is shown in (4). The result is a linear "design space," as shown in Fig. 2 and explained in [21],

$$V(\theta) = (1 - \cos(\theta))(1 + \beta \cdot \sin(\theta)), \qquad -1 \le \beta \le 1.$$
(4)

The task of the designer is now greatly simplified. No longer is the matching network constrained to a single set of distinct impedances, but to the extent that the given device technology can withstand the higher peak voltages, a degree of freedom has been introduced that can incorporate the movement of the matching network with frequency [30]. New high voltage breakdown device technologies such as gallium–nitride (GaN) are ideally suited to take advantage of these high peak voltage modes [31]; however, the continuum has been shown to be equally valid for more traditional GaAs and silicon technologies [24], [32].



Fig. 2. Class B/J design space in the impedance domain.

This freedom can be used to minimize the number of poles in the matching networks for a constant bandwidth, thereby minimizing loss and cost, or for the same number of poles the network can target a greater bandwidth. This can be key in even moderate bandwidth designs, where every additional filter pole introduces loss, degrading performance.

The same is true of the continuous Class F voltage waveform family [23] that establishes the same tradeoff between an expanded matching trajectory on the Smith chart and higher peak voltages.

III. LIMITATIONS OF CLASSICAL CONTINUOUS MODES

Fig. 2 highlights a significant limitation of the Class B/J design space. For every point on the fundamental impedance trajectory, there exists a singular point on the second harmonic plane that satisfies the original voltage equation (thus every fundamental point A, B, and C has a corresponding second harmonic A, B, and C). However, it can be shown that this second harmonic impedance must have no real part and that any deviation from the appropriate amount of reactance (either more or less) will produce a voltage waveform that attempts to "cross zero," violating a key constraint.

Fig. 3 shows the voltage waveforms that would theoretically be generated if the second harmonic reactance strays from the classical Class B/J stipulation. It is clear that straying by any amount from the ideal second harmonic impedance will introduce interaction with the current waveform via the device knee, thus greatly degrading the linearity.

In addition to the restriction on the second harmonic, Class B/J only allows for a v_{1r} value equal to unity. This means that for a given value of R_L (the load impedance extracted via the load line technique), the fundamental impedance must have a real value equal to R_L for the entirety of the circuit bandwidth; a difficult task when designing wideband matching networks [33]

$$R_L = 2 * \frac{V_{DSS}}{I_{DSS}}.$$
(5)

It is not clear to the PA designer how detrimental or beneficial it would be to introduce any more or less v_{1r} into the Class B/J voltage waveform, or to have an incorrect Z_{2F0} . Outside



Fig. 3. Voltage time-domain waveforms (*right*) versus their corresponding fundamental (Z_{1F0}) and second harmonic (Z_{2F0}) impedances (*left*), highlighting the effect of incorrect second harmonic reactance. Class B/J predicts a singularity when $v_{1r} = 1$.

of these constraints, the classical theory gives no guidance. It would be extremely useful to have access to a simple voltage waveform formulation that retains the freedom of the β term in the Class B/J formulation, but that is valid for any value of v_{1r} .

> IV. NEW VOLTAGE WAVEFORM AND THE DERIVATION OF CLIPPING CONTOURS

$$V(\theta) = (1 - \cos(\theta + \delta))(1 + \beta \cdot \sin(\theta + \gamma)),$$

-1 \le \beta \le 1; \le \delta, \gamma < 2\pi. (6)

As shown in [34] and [35], (6) is suggested as a solution to the problem of handling non-unity v_{1r} . Equation (6) has interesting properties that make it suitable for PA mode design.

- The introduction of two new phase shift operators, δ and γ, allow the sine and cosine terms to have both real and imaginary parts. This enables, through superposition of the two real parts, the v_{1r} term to be greater than or less than unity.
- 2) All of the waveforms generated by this equation "graze" zero. That is they never go below zero and all have a value of θ whereby $V(\theta) = 0$, as suggested in [21],

$$0 = 1 - \cos(\theta_{\text{zero}} + \delta)$$

$$\theta_{\text{zero}} = \cos^{-1}(1) - \delta$$

$$\theta_{\text{zero}} = -\delta.$$

3) By having three degrees of freedom (β, δ, and γ), it can be shown that by fixing v_{1r} and v_{1q} and solving the simultaneous equations, the formulation will yield a linear set of solutions versus the third degree of freedom.

Point 3 is key, as it suggests that solutions to (6) represent a boundary case. This boundary case we call the clipping contour. On one side of the boundary, waveforms will attempt to go below zero and on the other side, will never reach zero. This will be of critical importance for a designer attempting to manage interaction with the knee region.

A. Basic Clipping Contour Drawing Methodology

The Fourier series of (6) can be calculated and normalized to dc as follows:

$$v_{1r} = \frac{\beta \sin \gamma - \cos \delta}{1 - \frac{\beta}{2} \sin(\gamma - \delta)} \quad v_{1q} = \frac{\beta \cos \gamma + \sin \delta}{1 - \frac{\beta}{2} \sin(\gamma - \delta)} \quad (7)$$

$$v_{2r} = \frac{-\frac{\beta}{2}\sin(\gamma+\delta)}{1-\frac{\beta}{2}\sin(\gamma-\delta)} \quad v_{2q} = \frac{-\frac{\beta}{2}\cos(\gamma+\delta)}{1-\frac{\beta}{2}\sin(\gamma-\delta)} \quad (8)$$

$$v_{3r} = 0 \quad v_{3q} = 0. \tag{9}$$

It is important to note the following.

- Since the fundamental real voltage term has been normalized to dc, both the output power of the PA and η are governed solely by v_{1r}.
- The task of the second harmonic voltage is not to enhance power or η , but to produce a voltage waveform that does not degrade power, η , or linearity by clipping the current waveform.

Filter matching networks typically become more sensitive to component variation at higher frequencies. As a result, the typical design flow is, once a suitable network topology is selected, to tune the lower harmonics before the higher. It would be of greater use to the designer therefore to solve the above equations for the second harmonic, given a fixed fundamental. This result we term the "second harmonic clipping contour."

Mathematically we say for a given fixed fundamental voltage, and hence, a corresponding Z_{1F0} ,

$$\left[v_{1r}^a, v_{1q}^a\right]$$

There exists a set of solutions

$$\left[\beta^{A}, \delta^{A}, \gamma^{A}\right] = \left\{ \left[\beta^{1}, \delta^{1}, \gamma^{1}\right], \dots, \left[\beta^{n}, \delta^{n}, \gamma^{n}\right] \right\}$$

that result in the same values of fundamental voltage components v_{1r}^a and v_{1q}^a ; this is defined as the second harmonic clipping contour. For given fundamental matching conditions defined by v_{1r}^a , v_{1q}^a , a resulting set of unique solutions for the second harmonic exists that can be calculated using the matching free variable set

$$\begin{bmatrix} v_{2r}^{A}, v_{2q}^{A} \end{bmatrix} = \left\{ \begin{bmatrix} v_{2r}^{1}, v_{2q}^{1} \end{bmatrix}, \dots, \begin{bmatrix} v_{2r}^{n}, v_{2q}^{n} \end{bmatrix} \right\}$$
$$v_{2r}^{A} = \frac{-\frac{\beta^{A}}{2} \sin(\gamma^{A} + \delta^{A})}{1 - \frac{\beta^{A}}{2} \sin(\gamma^{A} - \delta^{A})}$$
$$v_{2q}^{A} = \frac{-\frac{\beta^{A}}{2} \cos(\gamma^{A} + \delta^{A})}{1 - \frac{\beta^{A}}{2} \sin(\gamma^{A} - \delta^{A})}.$$

It is then possible to compute the impedances of these second harmonic voltage components using the aforementioned fixed optimal current waveform and to plot this boundary, or clipping contour, on the Smith chart.

B. Optimizing Generation

In principle, if β is used as the swept parameter that maps out the clipping contour for a given set of values for v_{1r} and v_{1q} , (7) can be solved for δ and γ as β is varied between -1 and +1. The second harmonic components v_{2r} and v_{2q} can then be directly determined from (8) and the corresponding impedance locus plotted out.

It is possible to identify the matching set of three independent variables (β , δ , and γ) purely iteratively, computing the fixed harmonic (in this case, v_{1r} and v_{1q}) for a large number of randomly selected variations, then matching these computed values with a certain degree of tolerance to a preselected value. The collection of "matching" independent variables would then be used to generate the set of v_{2r} and v_{2q} values of the clipping contour.

In practice, to achieve an acceptable degree of accuracy while simultaneously achieving sufficient fundamental matches to show a smooth continuous contour on the Smith chart, approximately 10^5 calculations per independent variable are necessary. With three independent variables, this amounted to 10^{15} calculations per contour. Even for modern computers with hardware floating point support, this number of multiplication and trigonometric identities is cumbersome, taking tens of seconds per contour.

To yield a useful design tool, the calculation would ideally be instantaneous, enabling the designer to sweep across frequency and tune matching element values while updating the clipping contour in real time.

One possible method to minimize computational time would be to use numerical root-finding methods. These typically result in only one or possibly two orders of magnitude improvement in the calculation speed, their efficiency being dictated by the cost of computing their cost function. Ideally, we would analytically eliminate the redundant degrees of freedom, leaving only those required to plot the contour.

If we consider the equations for v_{1r} and v_{1q} in (7), it is possible to rearrange both with β as the subject

$$\beta = \frac{2\cos\delta + 2v_{1r}}{2\sin\gamma - v_{1r}\sin(\delta - \gamma)} \tag{10}$$

$$\beta = \frac{-2\sin\delta + 2v_{1q}}{2\cos\gamma - v_{1q}\sin(\delta - \gamma)}.$$
(11)

Subtracting (10) from (11) eliminates β ,

$$\frac{2v_{1q} - 2\sin\delta}{2\cos\gamma - v_{1q}\sin(\delta - \gamma)} = \frac{2\cos\delta + 2v_{1r}}{2\sin\gamma - v_{1r}\sin(\delta - \gamma)}.$$
 (12)

Multiplying both sides by the demoninator and rearranging for $sin(\gamma)$ leaves a numerator on the right-hand side that can be factorized by $cos(\gamma)$,

$$\sin \gamma = \frac{(-\cos\gamma)(v_{1r} + v_{1r}\cos^2\delta + 2\cos\delta - v_{1q}\cos\delta\sin\delta)}{2\sin\delta + v_{1r}\sin\delta\cos\delta - 2v_{1q} + v_{1q}\cos^2\delta}.$$
(13)

Dividing across by $\cos(\gamma)$ yields a tangential function of γ purely in terms of δ , that is the variable we will sweep to draw the contour (remembering that v_{1r} and v_{1q} are "fixed" and are thus known quantities)

$$\tan\gamma = -\frac{v_{1r} + v_{1r}\cos^2\delta + 2\cos\delta - v_{1q}\cos\delta\sin\delta}{2\sin\delta + v_{1r}\sin\delta\cos\delta - 2v_{1q} + v_{1q}\cos^2\delta}.$$
 (14)

Care must be taken when applying the inverse tan function as this can lead to angle ambiguities. The remaining variable β is found by substituting back into (10). A smooth contour can be drawn in just over 10^4 calculations using the closed-form equations.

It is important to note that (14) is only valid for the second harmonic clipping contour. To produce a solution for the "fundamental clipping contour," where v_{2r} and v_{2q} are the fixed variables, the process must be repeated starting with (8),

$$\beta = \frac{-2v_{2r}}{\sin(\delta + \gamma) + v_{2r}\sin(\delta - \gamma)} \tag{15}$$

$$\beta = \frac{2v_{2q}}{\cos(\delta + \gamma) + v_{2q}\sin(\delta - \gamma)} \tag{16}$$

$$\frac{v_{2q}}{\cos(\delta+\gamma) + v_{2q}\sin(\delta-\gamma)}$$

$$\frac{2v_{2r}}{\sin(\delta+\gamma) + v_{2r}\sin(\delta-\gamma)} \tag{17}$$

$$\sin \gamma = \frac{(-\cos \gamma)(v_{2q}\sin \delta - v_{2r}\cos \delta)}{v_{2q}\cos \delta + v_{2r}\sin \delta}$$
(18)

$$\tan \gamma = -\frac{v_{2q}\sin\delta - v_{2r}\cos\delta}{v_{2q}\cos\delta + v_{2r}\sin\delta}.$$
(19)

The existence of fundamental clipping contours was alluded to in [22] and [35], but only the case involving a purely reactive second harmonic. In addition, no method of generation was suggested (the figures shown were generated with intensive numerical optimization).

The remainder of this work will focus on the second harmonic clipping contour, as given by (14) and (10).

V. IMPEDANCE ANALYSIS

The second harmonic clipping contour formulation has the ability to predict the optimal second harmonic impedance space for any fundamental impedance, given information about the device parasitics and optimal load impedance (R_L) . Access to this information requires either the designer or the manufacturer to employ a suitable de-embedding methodology so as to extract the transistor parasitics. For higher power or high-frequency devices this is a non-trivial task. There is, however, increasingly widespread recognition by the device manufacturing and modeling community of the need for PA designers to access this intrinsic plane. As a result, package models are commonly now made available to designers and some manufacturers are providing "intrinsic ports" with their large-signal models. It is also important to note that the third and higher harmonics are assumed to be short circuited (i.e., have zero voltage component). This approximation can be justified on the basis that the assumed current waveform has a very low third harmonic component.

Fig. 4 shows the clipping contour computed with v_{1r} set to unity and no reactive component. This is the classical Class B condition that generates a sinusoidal voltage waveform with a Vmin of zero (for a device with zero knee voltage) when the second and all higher harmonics see a short circuit. The clipping contour demonstrates this fact by showing the only impedance on the Smith chart that does not generate a voltage waveform with a negative Vmin is a short circuit. Interestingly, there exists a space outside of the Smith chart that is "non-clipping."



Fig. 4. Clipping contour drawn for $v_1 = 1 + j0$ and an $R_L = 50 \Omega$. Second harmonic shown in the classical Class B position.



Fig. 5. Clipping contours along one side of the Class B/J design space. (a) Showing continuum. (b) Zoomed in.

This design space has typically been rejected because it is unrealizable with passive matching networks. Recently, active harmonic injection techniques have been used to investigate this impedance area [36].

Similarly, Fig. 5 shows clipping contours predicting the classical Class B/J design space. The clipping contours shown for each Z_{1F0} predict the single valid passive Z_{2F0} as given by the Class B/J equation. Again, for each Z_{1F0} point there exists a large area outside the Smith chart that can be exploited with active matching circuits. The key strength of the clipping contours, however, is the ability to predict the non-clipping second harmonic region in the presence of an arbitrary v_1 .

Fig. 6 shows the entirely new design space enabled by the clipping contour formulation. By trading off only half a decibel of output power (corresponding to a reduction in v_{1r} , and hence, $\operatorname{Re}[Z_{1F0}]$), the singular Class B/J design point opens to allow a variation of $j39 \ \Omega$ in reactance and 5.5 Ω of real variation in Z_{2F0} .

Perhaps more significant than the discovery of this new design space is the ability of the PA designer to analyze the sensitivity of this extended Class B/J design space to impedance mismatch. Unlike this ideal theoretical case of an infinitely "sharp" knee region, all real transistors display softer, more gradual transitions from the current limiting to the ohmic region. For the designer seeking maximum efficiency, but with limited linearity requirements, minor violations of the clipping contours is of secondary importance to achieving an optimal Z_{1F0} match. The



Fig. 6. Clipping contours showing the expanding design space as v_{1r} is reduced. (a) Z_{2F0} design space expands by reducing v_{1r} . (b) Showing the design space and the corresponding reduction in Puf, as defined in [1].

opposite is true of the designer seeking maximum linearity, who should seek to avoid the clipping case as much as possible.

In any case, it is clear from Fig. 6 that variation in the second harmonic reactance is less likely to induce clipping behavior than the introduction of real second harmonic. Fig. 5 shows that Z_{2F0} sensitivity decreases as the amount of reactive component in Z_{1F0} approaches zero.

Prior work has verified these clipping contours and their ability to predict regions of high efficiency using load–pull [34].

VI. DESIGN EXAMPLES

The suggested methodology for optimum exploitation of the clipping contours tool is as follows.

- 1) Choose a matching network topology with the appropriate movement of harmonic impedances over frequency.
- 2) Configure the network to optimally match the fundamental impedance.
- 3) Optimize the network to optimally match the second and higher harmonics.

A. Topology Choice

For a Class B/J matching network design, it is advantageous to exploit a key property of the transmission line; its tangential or oscillatory frequency response. The resulting clockwise impedance trace on the Smith chart, as demonstrated in Fig. 7, can be used to achieve the antiphased movement of fundamental and second harmonic impedances necessary for Class B/J operation.

Fig. 7 shows an initially acceptable Z_{1F0} trace behavior of a non 50- Ω transmission line with a 50- Ω terminating impedance on a 50- Ω Smith chart. The clockwise rotation can clearly be seen; however, the second harmonic comes back inside the Smith chart.

Replacing the terminating broadband load at the end of the transmission line with an ideal filter can reduce the impedance seen at the second harmonic. This shows how a transmission line terminated with a simple low-pass filter is an extremely effective Class B/J matching network.



Fig. 7. Simple transmission line network showing the clockwise circular movement with frequency.



Fig. 8. Mapping the effect of changing the transmission line terminating impedance at the second harmonic.



Fig. 9. Introducing a simple transistor output parasitic network.

Fig. 9 shows the network is robust in the presence of low amounts of parasitic degeneration. Looking at the Igen impedances beyond a simple parasitic network shows the relationship of antiphase Z_{1F0} and Z_{2F0} is maintained. The shift in matching impedances can be corrected by suitable modification of the filter that is also capable of reversing the curvature of the Z_{1F0} trace.

B. Deembedding and Optimum Network Design (Demonstrator *A*)

Using a Cree CGH40010F 10-W GaN device, a circuit was designed based on the selected topology (Fig. 10). The circuit targeted a fundamental band of 2–3 GHz and was tuned to optimize Z_{1F0} while minimizing the real part of Z_{2F0} , as shown in Fig. 11. The reactance ratio between the fundamental and second harmonic as specified by classical Class B/J theory was relaxed to achieve minimal real Z_{2F0} .

The final network was tuned to incorporate the device output parasitics, thus the size of the transmission line was reduced



Fig. 10. Ideal matching circuit (device drain at port 1).



Fig. 11. Matching impedances at the Igen plane showing Z_{1F0} from 2 to 3 GHz and Z_{2F0} from 4 to 6 GHz. Photograph of demonstrater A on right.



Fig. 12. Input matching impedances presented at the gate and transistor Z_{F0} conjugate match. Z_{F0} from 2 to 3 GHz, Z_{2F0} from 4 to 6, and Z_{3F0} from 6 to 9 GHz. Schematic of the input filter shown on the right.

from the theoretical 180° phase length. A surface mount inductor was used to supply the drain bias.

The input filter network (Fig. 12) was a simple transmission line and shunt capacitor to achieve flat gain over the design bandwidth. In addition, a shunt RC and a series R were added to maintain unconditional stability from dc to 6 GHz, the manufacturer stated maximum operating frequency of the transistor.

S-parameters of the packaged and unpackaged die were provided by the device manufacturer. By converting to ABCD matrices and applying simple matrix manipulation, S-parameters blocks for the package parasitics were extracted. The final deembedding step involved the use of an ideal inductance to model the bond wire, a wide section of transmission line to model the bonding pad, and an ideal capacitance to model the device drain–source capacitance. While this simple technique proved acceptable at the low gigahertz frequencies targeted by



Fig. 13. Simulated Igen dynamic load lines overlain on the simulated DCIV traces (a) and IV waveforms (b) across the operating band. Input power was 29 dBm. (a) Dynamic load line across frequency, (b) Igen IV waveforms showing managed interaction with the knee.

this design, the degree of error will be unacceptable at higher frequencies. Ideally, the cold FET parasitic extraction technique would be used to model the parasitics. The lack of an available device fixture prohibited use of this technique. A commercially available large-signal device model provided by Cree was used to verify the simple deembedding network.

The simulated Igen waveforms as extracted using the deembedding (shown in Fig. 13), conformed to the hypothesis of a voltage-controlled current source. Both voltage and current were non-negative for the whole of the cycle. The voltage waveform did not violate the knee voltage condition and the waveforms showed clear similarities to theoretical Class B/J.

When targeting high efficiency, minimizing the loss of the matching network is as important as engineering the optimal impedance environment. The transmission loss (S21) of the circuit shown in Fig. 10 is plotted in Fig. 14. Careful attention was paid to the tuning of the filter to ensure the cutoff frequency remained acceptably above the maximum fundamental frequency of operation and the use of lossy surface mount components was minimized. A small amount of roll-off with frequency was observed both in simulation and later in measurements.

As previously stated, clipping contours predict a large degree of flexibility in the Z_{2F0}/Z_{1F0} reactance ratio. Fig. 15 shows how this ratio was allowed to vary over the targeted fundamental frequency range, compared to the ideal Class B/J ratio.

Key to the design of this network was the second harmonic clipping contour tool. Variation in Z_{2F0}/Z_{1F0} reactance was permitted to the extent that the clipping contour condition was not strongly violated. The design targeted high η , thus some violation of the clipping contour was deemed acceptable.

Fig. 16 shows that a small reduction in fundamental impedance (compared to the predicted R_L) produced enough



Fig. 14. Simulated matching network loss (including parasitic network).



Fig. 15. Simulated ratio of Z_{2F0}/Z_{1F0} reactance, showing the ideal Class B/J value overlain.



Fig. 16. Clipping contours calculated over frequency from the simulated output matching networks Igen impedances.

design space at the second harmonic to allow the circuit to follow the clipping contour.

The circuit was fabricated using a Rogers Corporation RT5880 Duriod substrate (508- μ m thick) with a thick clad aluminum back coating for physical robustness and optimal thermal performance.



Fig. 17. Measured output power versus frequency for a constant input power (29 dBm).



Fig. 18. Measured versus frequency for a constant input power (29 dBm).

The output matching network did not use external capacitors to maximize the circuit Q and attempt to reduce fabrication variation due to human error.

C. Demonstrator A Measured Results

All of the following results are measured with an input power of 29 dBm, a drain voltage of 28 V, and a gate voltage of -2.8 V.

The circuit achieved at least 8.5-W output power over the whole of the design band and a maximum output power of 10.4 W at 2.8 GHz. The power rolled off above 2.9 GHz, as shown in Fig. 17. The performance extended well below the design band, suggesting the efficacy of the selected topology.

Drain efficiency followed the trend of output power, with a nominal value of 60% from 1 to 2.9 GHz. The predicted value shown in Fig. 18 was calculated using an extremely simple knee model.

$$I_k(\theta) = I(\theta) * \log_2 \left(\frac{V(\theta)}{V \text{knee}} + 1\right)^{0.71}.$$
 (20)

This knee model was applied to the current waveform if the clipping contours algorithm predicted the voltage would clip the current. Both waveforms were then passed through the Fourier transform and the efficiency was calculated, demonstrating once more the power of the clipping contour tool and the importance



Fig. 19. S21 at a constant input power (29 dBm).



Fig. 20. Measured ACPR with single-carrier WCDMA at a constant input power (29 dBm). No attempt has been made to linearize the circuit.

of avoiding major current waveform modulation in achieving high-efficiency operation.

Previous work has shown this device capable of up to 70% η under certain conditions. This design was rather conservative with the selection of R_L to expand the clipping contour design space, thus limiting the efficiency that could be achieved. A higher value of R_L would generate less output power because of the lower Imax, but would enable a lower minimum voltage and correspondingly a higher efficiency. This highlights the importance of choosing an appropriate R_L value to achieve optimal performance.

Large-signal gain is also high for the device (Fig. 19), an advantage of operating in a (nominally) uncompressed mode.

Fig. 20 demonstrates a representative linearity measurement with a 5-MHz single carrier WCDMA signal (3.84 chips/s, 0.22 raised root cosine filter). The presented numbers are raw figures from the device without any attempt at linearization. The amplifier shows a nominal ACPR 30 dB below the carrier frequency from 1 to 3 GHz.

Due to the wide bandwidth of the device, two separate preamplifiers were necessary; Preamplifier A was used to measure 1–2.5 GHz and Preamplifier B above 2.5 GHz. Fig. 20 shows separate traces for each of the preamplifiers. Preamplifier B degraded the signal slightly more than the Mini-Circuits, consequently the true linearity figure of the clipping contours amplifier may be lower.



Fig. 21. Clipping contours demonstrator B. Igen impedances from 2 to 3.5 GHz for Z_{1F0} is shown on the left, as well as harmonics. Z_{2F0} shows large real part both at the lower and upper band edges. Circuit photograph is on the right.



Fig. 22. Clipping contours from demonstrator B's simulated Igen impedances.

D. Comparison Demonstrator B (Violating the Clipping Contour Condition)

A similar amplifier (shown in Fig. 21) was built, this time violating the clipping contours condition at both the top and bottom of the band.

This second demonstrator circuit used a 20- Ω resistor in the output matching network to induce loss at the second harmonic while keeping Z_{1F0} flat and maintaining low loss.

This design strongly violated the clipping contour line at both the lower and upper edges of the design bandwidth, as shown in Fig. 22. It was expected to see degradation in performance at the upper and lower edges and a peak in performance mid-band.

Fig. 23 shows the strong correlation between the clipping contours theory and the measured results. Both upper and lower band edges experience a significant reduction in performance. The performance at the mid-band peak was better than demonstrator A; this is largely attributed to a marginally higher R_L .



Fig. 23. Measured and predicted [from clipping contours and (20)] η for demonstrator B. Note the different frequency scale to Fig. 18.

VII. CONCLUSION

A novel continuous mode voltage equation first presented in [34] has been expanded and a fast efficient method for the calculation of second harmonic clipping contours has been derived.

The clipping contours have been shown to be an extension of classical Class B/J theory, and as a result, predict the singular Class B/J conditions. The power of the resulting clipping contours, especially their role in identifying mode sensitivity to impedance mismatch, has been highlighted.

A design example has shown how second harmonic clipping contours can be integrated into a traditional design flow. Two demonstrator circuits were designed, fabricated, and measured. The first attempted to obey the constraints of the clipping contours and the second made a deliberate attempt to violate them. Both circuits used the same transistor and attempted to maintain all other variables constant.

The non-clipping contour violating circuit was capable of at least 8.5 W from 1 to 2.9 GHz and 9 W from 1 to 2.2 and 2.7 to 2.9 GHz. The efficiency was approximately 60% from 1 to 2.9 GHz with a minimum value of 56.8% at 2 GHz. The linearity was tested under single carrier WCDMA and achieved an ACPR of at least -30 dBc from 1 to 2.9 GHz.

The clipping demonstrator exhibited performance degradation closely correlated to the extent to that the clipping contour condition was violated.

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