The Wireless Workhorse

Hua Wang, Shouhei Kousai, Kohei Onizuka, and Song Hu

The ever-growing demand for higher data rates, power efficiency, and robust operations poses increasingly stringent performance requirements on wireless transceiver systems. This is particularly critical for mobile devices in both commercial and defense applications, where improving system size, weight, and power metrics and extending the battery lifetime are often the primary concerns. The power amplifier (PA) serves as the interface between the RF transmitter

Hua Wang (hua.wang@ece.gatech.edu) and Song Hu (husong@gatech.edu) are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, United States. Shouhei Kousai (shouhei.kousai@toshiba.co.jp) and Kohei Onizuka (kohei.onizuka@toshiba.co.jp) are with the Center for Semiconductor R&D, Toshiba Corporation, Japan.

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system and the antenna and is often considered one of the most critical building blocks in a wireless transceiver. This is because the PA's performance has critical impacts on multiple major transmitter metrics, including the output power level, power efficiency, bandwidth, and signal fidelity, and therefore governs the overall quality of service (QoS) of the wireless link [1], [2]. Moreover, due to their large-signal and high-power operations at RF frequencies, PAs often encounter unique design challenges and tradeoffs that deserve special attention [3].

What Are the Key PA Performance Metrics?

Table 1 summarizes several key PA performance metrics, how they impact transceiver system performance, and the PA design techniques used to improve these metrics.

The PA output power determines the transmitter output power level, which is an important aspect in estimating the wireless system link budget and the effective communication range [1]. The efficiency of the PA determines its dc power consumption, i.e., the battery lifetime in mobile devices. It also sets the thermal handling requirement on the packaging solutions because the dc power consumed by the PA is either transmitted as the desired RF signal or wasted as unwanted heat dissipation [5]–[7]. PAs operating at high power levels, e.g., +20 dBm and above, often dominate the power consumption of the entire transceiver RF front end in a mobile device. Therefore, the PA's efficiency will largely govern the energy efficiency of the whole wireless link, and this is often denoted by the picojoules/bit performance for energy-efficient wireless links.

Besides these power-related metrics, the linearity of the PA is also an important performance aspect and is particularly critical in the amplification of complex modulated signals with nonconstant envelopes. In these applications, the PA nonlinearity behavior may corrupt the amplitude modulation (AM) signals through its AM–AM distortion and the phase modulation (PM) signals via its AM–PM distortion. These "in-band" nonlinearities distort the transmitted constellations, cause a degraded error vector magnitude (EVM) and bit error rate, and eventually deteriorate the QoS of the wireless link [3], [4]. Moreover, the nonlinear PA behavior also alters the constellation trajectories and generates undesired intermodulation tones. Such "out-of-band" distortion may cause transmitter output spectrum regrowth, violate the spectrum mask compliance, and result in the jamming of other wireless links in a dense electromagnetic environment [3], [4].

In parallel, there has recently been increasing interest in improving the PA performance robustness against antenna load variations [8]–[10]. This is especially relevant for commercial mobile devices and field-deployable systems in defense applications. The wireless transceiver systems in these applications often

TABLE 1. PA performance metrics, impacts on transceiver system performance, and corresponding design techniques.

PA Metrics	Transceiver Performance	PA Design Techniques
Output power	Link budget	Power combining [16], [61], [62]; device stacking [63], [64]
Peak power efficiency	Power consumption/battery life	Switching-mode operation [3], [65]
Back-off power efficiency (large peak-to-average power ratio)	Power consumption/battery life	Doherty [33], [36], [38]; envelope elimination and restoration [66]–[69]; envelope tracking [18], [70]–[73]; class-G [28], [32]; out-phasing [42]–[49]; load modulation [30]; hybrid mode [39], [45]
Signal fidelity/linearity (amplitude/phase)	Data error rate/spectrum compliance	Digital predistortion [21], [22], [51], [52]; feed-forward [54]; feedback [53], [74]
Noise floor and transmitter leakage	Spectrum compliance	Finite impulse response filter [75], [76]; feed-forward cancellation [77]–[79]
Bandwidth	Data rate/frequency agility	Wideband matching [14], [83]–[85]; continuous-mode switching PA schemes [80]–[82]
Robustness against antenna mismatches	Wireless link robustness	Load detection and tuning [56]–[59]; wideband matching [14], [83]–[85]; balanced amplifier [15]
Module size and cost	Transceiver system size, cost, and packaging complexity	Multichip-module, III-V compound device chips, full CMOS integration

experience time-varying electromagnetic radiation environments, necessitating specialized PA designs that are inherently insensitive to antenna impedance mismatches or capable of autonomously detecting and calibrating such load variations.

In addition, other PA performance metrics, such as bandwidth, noise floor, size, and cost, also require judicious design considerations to meet the application specific requirements [3], [4].

Unique Advantages of Silicon-Based PAs

Traditionally, III-V compound semiconductor devices, such as GaAs heterojunction bipolar transistors (HBTs), have been the dominant technology choice for high-power wireless PA applications, e.g., mobile handsets, due to their superior device performance. The intrinsic large bandgaps and device breakdown voltages support high-power-handling capabilities in the III-V compound device technologies. They also provide low-loss substrates, high-quality metal options, and through-substrate vias that enable high-performance passive designs, minimum device-to-ground impedances, and a high thermal conductivity. Certain compound processes, for example, GaAs HBTs, also offer superb cost-effectiveness when being manufactured in a mass production [11], [12].

The multichip module (MCM) is a popular approach for assembling an HBT PA. Typically, it is composed of a dedicated HBT die with optimized power transistors and a complementary metal–oxide–semiconductor (CMOS) integrated circuit (IC) chip as the PA controller, and its passive networks are implemented using discrete components or integrated passive devices (IPDs). This solution often achieves an excellent cost and performance tradeoff. However, the required footprint is commonly an issue for the HBT/MCM solution. Thus, the RF PA front end may occupy a substantial area compared with the RF transceiver. In addition, due to recent increasing demand for multiband operation [13] and immunity to the antenna proximity effect [8]–[10], wideband matching network [14], and quadrature balanced topologies [15] are employed in HBT PA designs to achieve robust operation against frequency variations and antenna load mismatches—though at the expense of a possibly larger footprint and a compromised power efficiency.

On the other hand, silicon-based PAs, particularly CMOS PAs, have recently emerged as a competitive PA solution in low-cost, high-volume markets. Silicon-based PAs often feature one-chip, fully integrated solutions, resulting in a smaller footprint and a significantly simplified front-end assembly process [16]. Further, CMOS PAs naturally lend themselves to complete system-on-chip (SoC) solutions, which are now becoming one of the technology trends in multiple wireless markets. Most importantly, CMOS platforms offer unparalleled on-chip analog/digital signal computation and processing, which can be exploited to substantially enhance the large-signal RF PA performance, while still offering a low cost and low overhead [23], [32], [36]–[39]. Note that these analog/digital signal processing techniques may perform automatic in situ PA performance enhancement [55], [59] or operate together with the baseband processors, as in conventional digital predistortion (DPD) techniques.

Leveraging all the unique advantages of CMOS to benefit PA performance may eventually result in a total paradigm shift in the PA design methodology and design space. As a result, advanced CMOS PA designs have now expanded their scope from a standalone RF circuit building block to a complex mixed-signal/mixed-mode RF system with orchestrated collaborations among analog, digital, and large-signal RF operations.

In practice, a fundamental challenge in PA designs is the direct tradeoff between PA efficiency and linearity performance [3], [4]. The increasing demand on the data rate leads to a wide use of spectrum-efficient modulations, which often require nonconstant envelopes and large peak-to-average power ratios (PAPRs). Thus, PAs often operate in the power back-off mode to accommodate the PAPR and provide sufficient AM–AM and AM–PM linearity. However, most PAs are designed to achieve peak efficiency only at the maximum output power. This means that power back-off operations will substantially degrade the average efficiency of the PA, defined as

$$\text{average } \eta = \int \eta(P_{\text{out}}) \cdot \text{PDF}(P_{\text{out}}) dP_{\text{out}}, \tag{1}$$

where $\eta(P_{\text{out}})$ is the PA efficiency at the output power levels P_{out} and $\text{PDF}(P_{\text{out}})$ is the corresponding probability density function (PDF) for the envelope modulation [Figure 1(a)]. For a given modulation scheme, PA efficiencies at both peak and back-off power levels jointly determine the averaged efficiency, which governs the actual dc power consumption and the battery lifetime of mobile devices. Alternatively, a reduced power back-off level may enhance PA efficiency but also lead to degraded in-band/out-of-band linearity due to deteriorated AM–AM/AM–PM distortions or even signal clipping [18].

The analog techniques and digital computations in CMOS processes can be exploited to address this PA efficiency–linearity tradeoff challenge. A practical strategy is first to explore innovative PA architectures that enhance PA power efficiency and then utilize various in situ analog/digital circuit techniques to improve PA linearity performance.

CMOS digital PAs, i.e., digital PAs (DPAs) or RF power digital-to-analog converters (DACs), can potentially offer superior peak efficiency and support complex modulation schemes [19]. Each DAC power cells operates as a switching PA for high efficiency. In a polar PA architecture, a proper number of power cells

can be turned on or off to "synthesize" the real-time envelope modulation, and the phase-modulated carrier can be used to drive the RF power DAC. Note that the efficiency of a basic CMOS DPA degrades during power back-off in a way that is similar to what occurs in a class-B PA [17]. While advanced PA architectures, such as class-G supply switching, supply modulation, Doherty, and outphasing, can be employed to enhance PA back-off efficiency in practice, these efficiency-enhancing PA architectures may cause linearity degradations with substantial AM–AM and AM–PM distortions. Thus, the analog/digital signal computation in CMOS can be utilized to enhance the linearity performance [36], [39], [55]. In parallel, employing appropriate analog/digital techniques may achieve on-chip complex load mismatch measurements and enable in situ load compensations [55], [59].

The purpose of this article is to review recently reported CMOS PA architectures that exploit mixed-signal (analog/digital) techniques to substantially improve PA performance. We will focus on PA efficiency, linearity, and load robustness, as they are the key metrics in many wireless systems and may benefit most from such mixed-signal operations. We explicitly exclude any detailed discussions of classic DPD techniques, since such matured techniques have been extensively covered elsewhere [21], [22], and they can often serve as an orthogonal PA linearity enhancement solution. In this article, we first present several exemplar DPA topologies for efficiency and linearity enhancement. Next, we demonstrate several recent PA designs that employ analog and/or digital techniques to augment classic PA architectures. Then, we introduce a recently reported PA architecture with a self-contained feedback linearization loop, which performs in situ PA linearization without any computation in the digital back-end. Finally, we consider PA designs with auxiliary analog circuits and digital reconfigurability for enhanced antenna load robustness.

The proposed mixed-signal PAs can be readily extended to multimode/multistandard wireless transmitters. However, addressing broadband high-data-rate applications, such as those meeting the 4G standards or millimeter-wave transmission requirements, may result in new challenges because the high data rates in these applications create demanding requirements on the analog bandwidth and/or the digital sampling rate for mixed-signal PAs. To this end, novel design techniques, such as in-phase/quadrature (Cartesian) PA architectures, can substantially reduce the required bandwidth [86]–[88]. Similarly, employing mixed-signal PAs in carrier aggregation systems also deserves special design consideration because some of the mixed-signal PA architectures introduced here, e.g., down-conversion-based PA closed-loop linearization [59], may not apply directly.

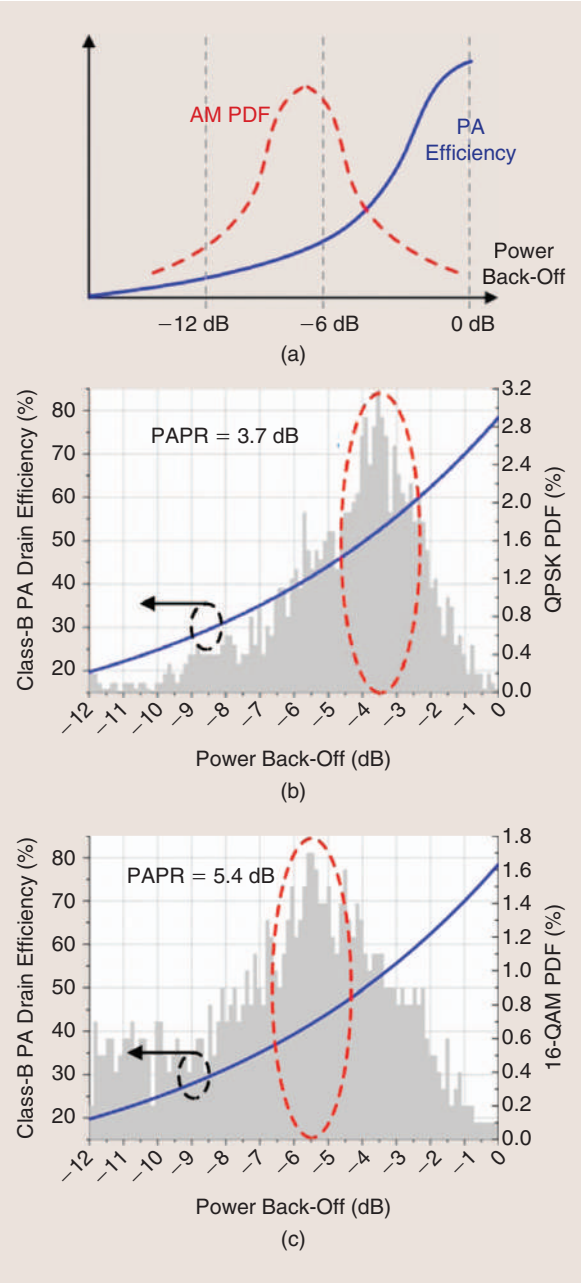

Figure 1. *(a) PA efficiency degradation at the power back-off and the PDF of the AM. (b) The amplitude PDF of a quadrature phase-shift keying (QPSK) signal (PAPR = 3.7 dB). (c) The amplitude PDF of a 16-quadrature AM (QAM) signal (PAPR = 5.4 dB). A class-B PA back-off efficiency curve is also plotted in (b) and (c).*

Digital PA Topologies (RF Power DACs) for Efficiency and Linearity Enhancement

DPAs and Digital Power Mixers

The DPA concept was first introduced by Staszewski et al. [19], and its basic polar configuration is shown in Figure 2(a). The amplitude of the PA output is synthesized by activating a proper number of unit PA cells. In advanced CMOS technologies, the number of

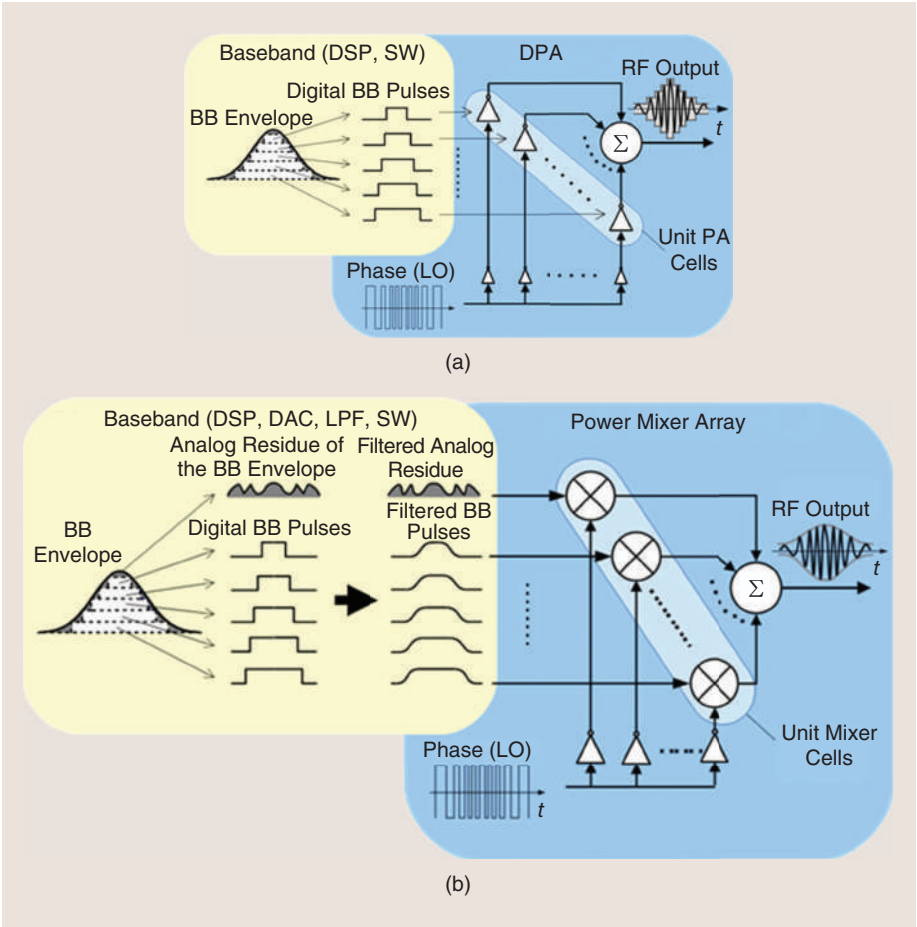

Figure 2. *Block diagrams of (a) a typical DPA and (b) a power mixer array with mixed-mode amplitude interpolation. DSP: digital signal processor; SW: switch matrix; BB: baseband; LPF: low-pass filter.*

activated unit PA cells can be controlled dynamically to produce wideband amplitude-modulated signals. A phase-modulated local oscillator (LO) signal is applied to drive the unit PAs. Thus, the PA operates in a polar fashion to include both AM and PM signals. The DPA can be highly efficient, as the unit PA cell can be implemented as an efficient switched-mode PA. Several major advantages, including a small feature size, easy integration into the transceiver ICs, high efficiency, and high flexibility/reconfigurability, make the DPA very attractive in CMOS implementations. Various DPA designs have been reported to extend the output power, linearity, and bandwidth [17]. However, DPAs typically suffer from limited dynamic range of the output power and the unwanted out-of-band spectrum emission due to aliasing and quantization noise.

A power mixer array architecture is reported to address these challenges [23]. Figure 2(b) illustrates a power mixer array as compared with a DPA. In the conventional DPA, polar modulation is employed, and the amplitude signal is synthesized digitally by turning on a proper number of unit PA cells, shown in Figure 2(a). This results in a limited output power range and quantization noise due to the finite weighting of the least significant bit (LSB) as well as signal aliasing by the zeroth-order hold signal reconstruction, leading to the potential noise floor and out-of-band spurs of DPAs. Moreover, for a frequency-division duplex (FDD) system, the resulting transmitter noise and spurs may fall into the receiving band and cause jamming.

The power mixer array fundamentally reduces DPA noise and spurs by employing a novel mixed-mode amplitude interpolation scheme [Figure 2(b)], [23]. First, the baseband digital pulses are filtered, i.e., pulse shaped, so that the interpolation spurs are largely suppressed. In parallel, an analog residue path is introduced to augment the digital amplitude synthesis [23]. This analog residue provides the amplitude signal between the discrete digitized amplitude levels, which enhances the fidelity of the amplitude interpolation and suppresses both the quantization noise and the sampling images [Figure 2(b)]. In addition, this analog residue path extends the PA's output power range, since it can amplify a small baseband analog signal to realize an output power level substantially lower than one LSB of the binary DPA cell array.

This power mixer architecture is implemented in a standard 130-nm bulk CMOS process with a chip area of 1.6 mm × 1.6 mm [Figure 3(a)]. It achieves a broadband operation with its peak output power of +31.4 dBm and its peak power added efficiency (PAE) of 43% [Figure 3(b)]. The mixed-mode operation allows the power mixer to achieve a >100-dB output power range with EVM better than 5% for a 16-quadrature amplitude modulation (QAM) signal [Figure 3(c)]. The measured output spectrum shows the reduced close-in transmitter output noise and the suppressed aliasing signals using the analog residue path (Figure 4). The power mixer array can produce accurate AM signals from the watt level down to −75 dBm, achieving the state-of-the-art output dynamic range among reported DPAs.

The power mixer concept can be extended to the millimeter-wave frequency range [24]. Compared with a classic heterodyne transmitter [1], the power mixer performs modulation, upconversion, and power

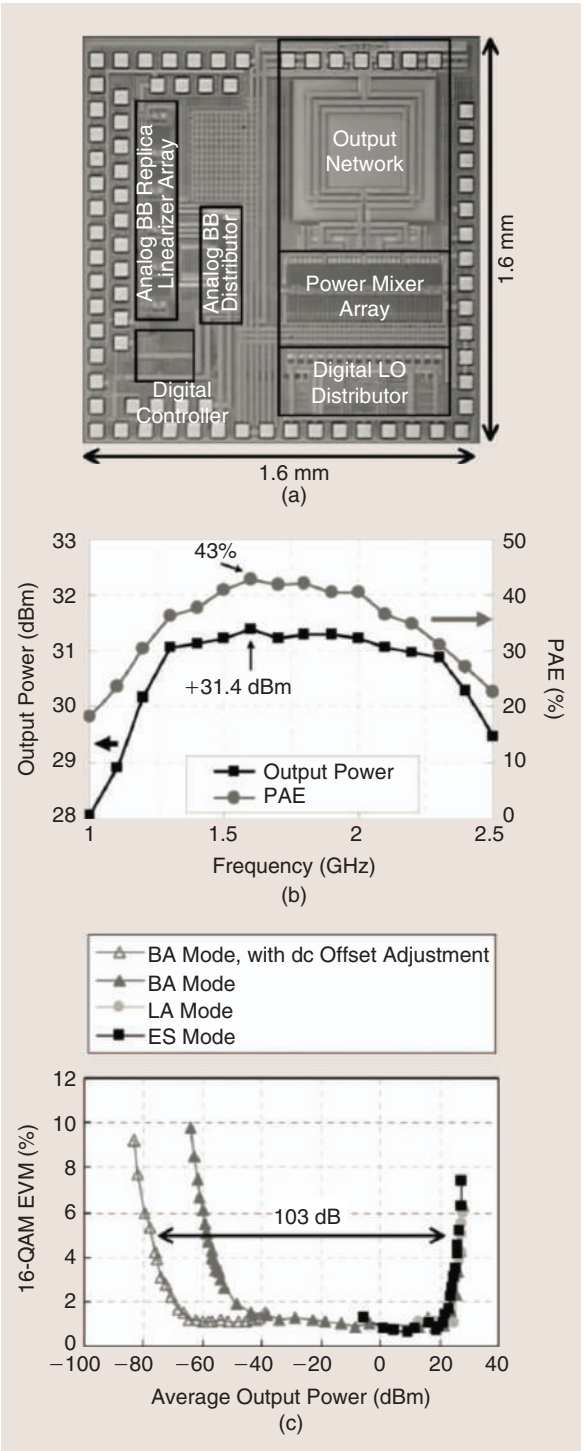

Figure 3. *(a) A microphotograph of a proof-of-concept chip design for a power mixer, (b) PA saturated output power and PAE versus carrier frequency, (c) and the average output power range of an amplified 16-QAM signal versus the EVM [23]. BA: baseline analog; LA: linearized analog; ES: efficient segmented.*

amplification all within the same block. Therefore, the additional power of the upconversion mixer and the area overhead of the mixer-PA matching networks can be directly eliminated by employing the power mixer architecture.

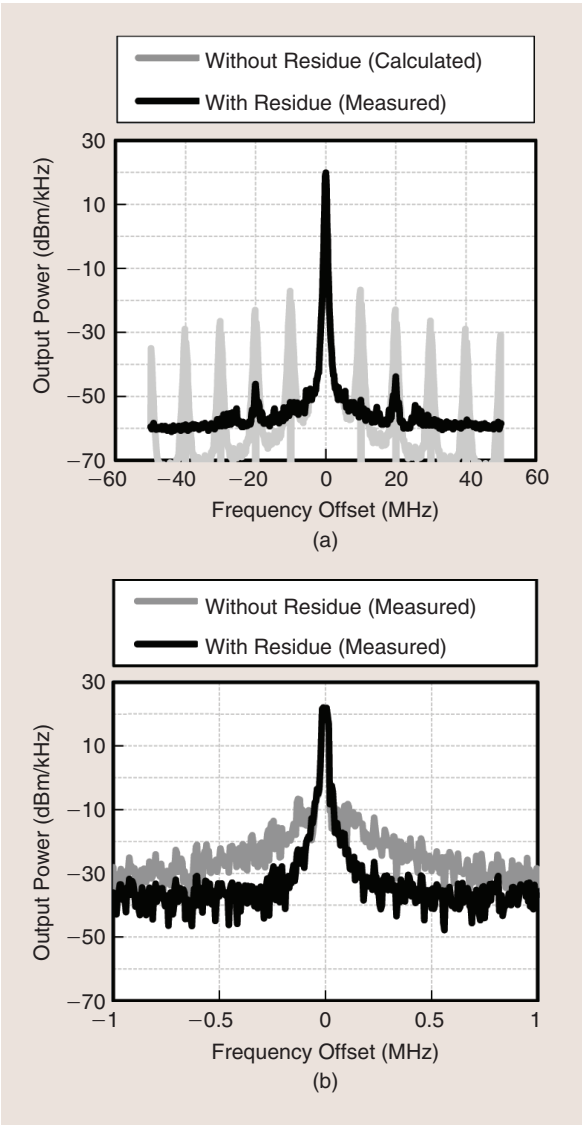

Figure 4. *Measured output spectrum of the power mixer array with (a) the reduced out-of-band spurs and (b) the reduced close-in noise floor [23].*

Switched Capacitor DPAs

Switched capacitor topologies have been widely used for filtering and voltage conversions in CMOS analog circuits [25]. Recently, a digital CMOS PA architecture based on a switched capacitor topology (SCPA) is demonstrated [26]. The PA core is composed of a capacitor bank, matching network, and a CMOS switch array to dynamically short the bottom plates of the capacitors to V_{DD} or ground [Figure 5 (a)]. The output power level is controlled by the ratio of the capacitors connected to V_{DD} and those connected to ground, while the PA output phase is determined by the zero-crossings of the phase modulated switching signal at the RF carrier frequency.

One major benefit of this SCPA topology is that the output level is precisely defined by the capacitance ratios, which can be well-controlled in advanced CMOS processes. In comparison, other reported DPAs often

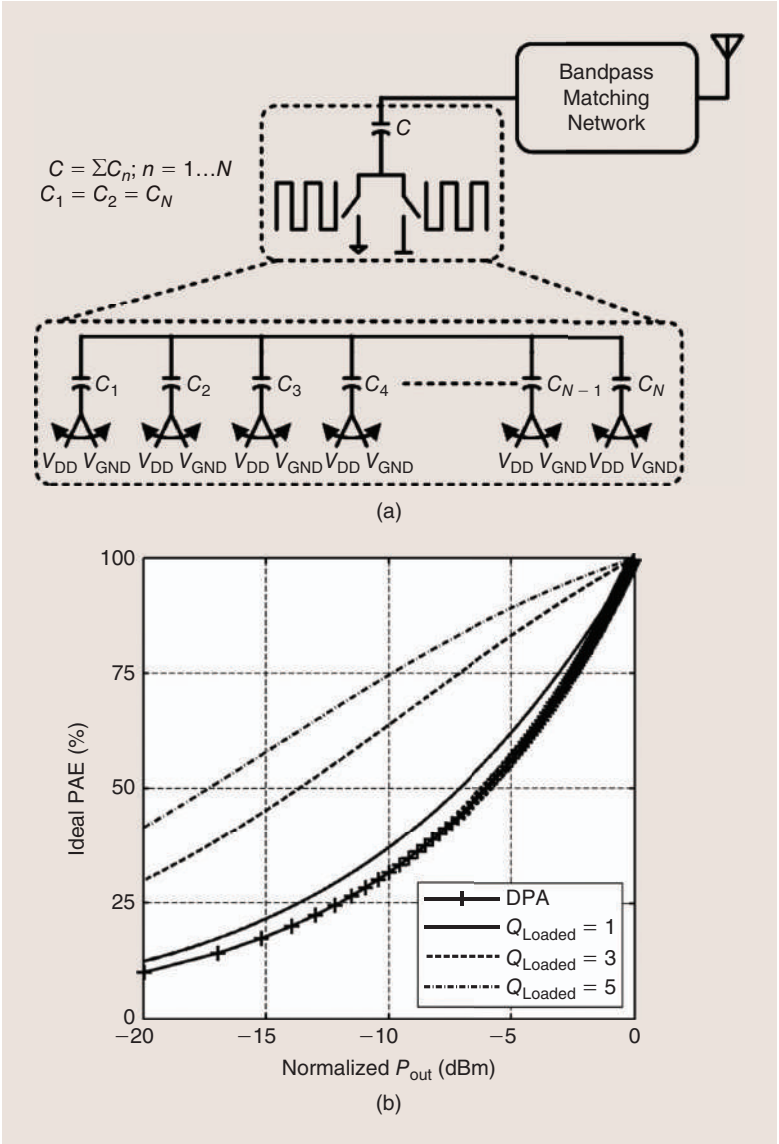

Figure 5. *(a) The SCPA topology and (b) ideal back-off efficiency curves for the SCPA and a class-B PA [26].*

require extra bits for sufficient linearity compensation. With its high-accuracy output amplitude interpolation, this SCPA topology also relaxes the requirement on the DPD algorithm. Moreover, the total capacitance of the switched capacitor bank stays constant regardless of the switching; this allows the same output matching network to be used with no need for amplitude dependent compensations [26].

The back-off efficiency characteristics of the SCPA topology are determined by the ratio of the energy transferred to the load versus the energy discharged through the bottom plates during the switching. Note that the theoretical SCPA back-off efficiency actually outperforms that of a class-B PA [Figure 5(b)]. The quality factor Q_{loaded} is defined by the optimum load resistance R_{opt} and the total capacitance C, assuming that the latter is resonated out by the matching inductor L. The quality factor Q_{loaded} can be expressed as

$$Q_{\text{loaded}} = \frac{2\pi fL}{R_{\text{opt}}} = \frac{1}{2\pi fCR_{\text{opt}}}. \quad (2)$$

The ideal PAE of an SCPA can be described as

$$\text{PAE}_{\text{ideal}} = \frac{4n^2}{4n^2 + \frac{\pi n(N-n)}{Q_{\text{loaded}}}}, \quad (3)$$

where N and n denote the total number of the unit capacitors and the number of capacitors actually in switching, respectively. In practice, the parasitic capacitances of the switches, drivers, and clock distribution network also affect the SCPA's power efficiency. In addition, the unbalanced impedances of p-type metal–oxide–semiconductor (PMOS) and n-type metal–oxide–semiconductor (NMOS) switches may introduce extra AM–AM and AM–PM distortions to the PA output, which then requires additional linearity enhancement.

A test chip designed in a 90-nm CMOS process with a chip area of 1.4 mm × 0.7 mm is shown in Figure 6(b) [26]. It achieves 45% peak PAE and +25.2 dBm output power at 2.2 GHz [Figure 7(a)]. The designed Q_{loaded} is around 2 for a broadband operation, and the switching code word has a 6-bit resolution to satisfy IEEE 802.11g for orthogonal frequency-division multiplexing (OFDM) EVM and spectrum mask requirements. Up to 50° AM–PM distortion is measured, which requires an extra phase DPD technique for linearization. An excellent average PAE of 27% is demonstrated for an IEEE 802.11g 64-QAM signal. The measured EVM is 2.6% root mean square (rms), which well satisfies the IEEE 802.11g OFDM EVM specification of 5.6% rms [Figure 7(b)]. A higher sampling frequency can be applied to suppress the unwanted sampling spurs. The PA output noise at the close-in frequencies can also be improved by a better alignment of the AM and PM signal paths with synchronized signal generators. The measured amplitude achieves a ±3 LSB integral nonlinearity and a ±0.5 LSB differential nonlinearity as an RF-DAC at the peak output power [26].

More recently, a combination of SCPA and class-G supply modulation was also demonstrated [27]. The class-G supply modulation is a PA back-off efficiency-boosting technique by setting the supply voltages with multiple discrete levels [28]. The test chip employs a two-level class-G topology and is fabricated in a 65-nm CMOS process with 1.4 mm × 1.2 mm chip area.

This PA operates at 2.15 GHz and achieves a very competitive PAE (average) of 33% when amplifying an IEEE 802.11g 64-QAM OFDM signal.

Inverse Class-D PA and Dynamic Load Impedance Modulation

DPAs typically employ high-efficiency switching PAs as the power cells in the output PA core. Class-D and class-E PAs are well known schemes with a theoretically 100% drain efficiency (DE) as well as practical design challenges. For example, a basic CMOS class-D PA functions as a broadband inverter driver, which may suffer from substantial power loss due to charging and discharging the device output parasitic capacitors. On the other hand, a class-E PA requires judicious tuning of the output network together with the switching duty cycle.

An inverse class-D (D^{-1}) PA is demonstrated as an attractive solution to implement DPA power cores [29]. "Inverse" here denotes the fact that the drain voltage and current waveforms of such a PA scheme are actually complementary to those of a basic class-D PA. More specifically, in a class-D^{-1} PA the drain voltage has a half-wave rectified sinusoidal waveform, and the drain current has a square-wave waveform (Figure 8). In comparison, the basic class-D PA generates a square-wave drain voltage and a half-wave rectified sinusoidal output current. The class-D^{-1} PA can also be viewed as a current mode dual scheme of the voltage-mode class-D PA. The class-D^{-1} PA can utilize a parallel LC tank with the load resistor as the output tuned load; this configuration absorbs the parasitic drain capacitances of the switching power devices and minimizes the power loss. The operation of a class-D^{-1} PA requires constant current biasing sources. These current sources can be effectively replaced by a dc feed inductor L_{dc} [Figure 9(a)]. Moreover, the device output capacitances can be carefully designed together with L_{dc} to control the second-order harmonic signals. In practice, the class-D^{-1} PA's output matching can be implemented as a transformer based network, and the simulation results confirm the desired output waveforms for gigahertz operations [Figure 8(b)].

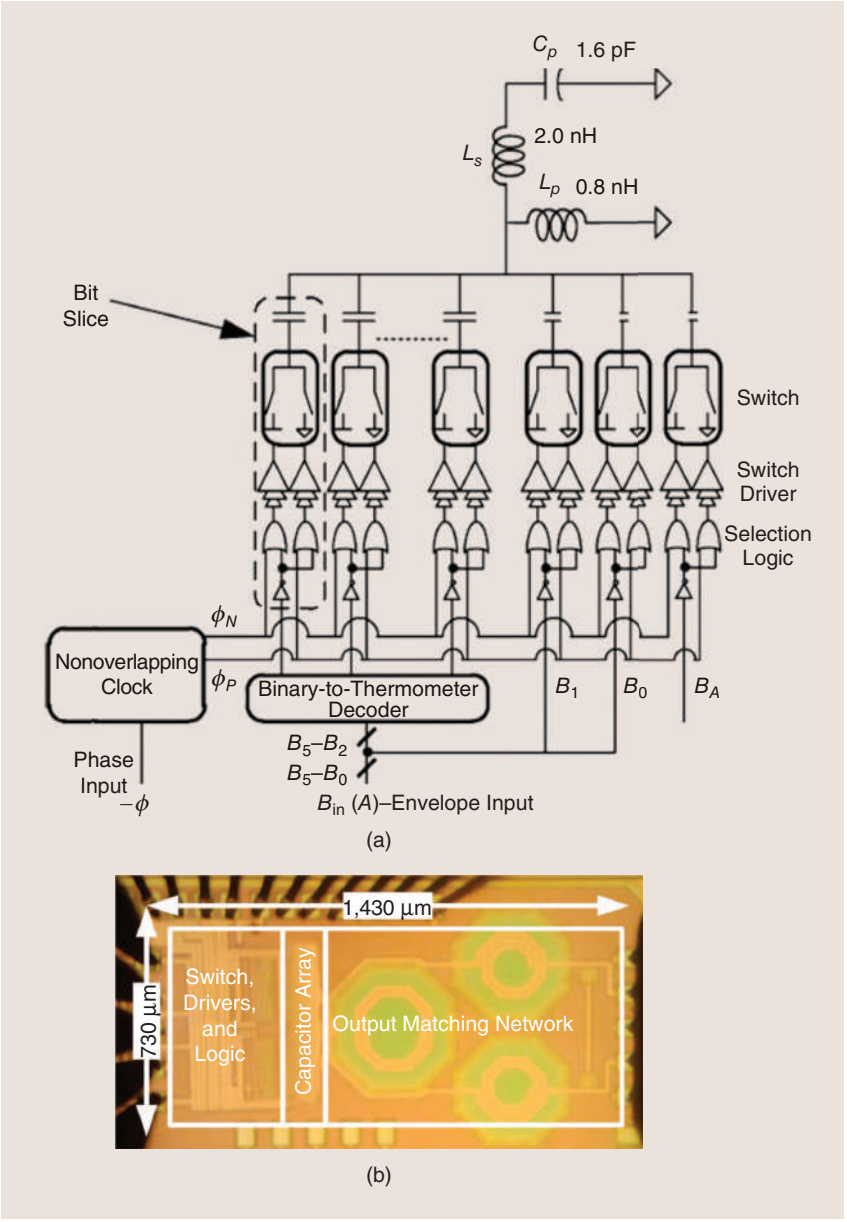

Figure 6. *(a) The overall schematic of an SCPA and (b) a microphotograph of a test chip [26].*

The class-D^{-1} PA is demonstrated in an RF digital polar transmitter [29]. The AM is achieved by enabling segmented power transistors, which are composed of 15 thermometer-coded PA cells for the four most significant bits and four binary-coded PA cells for the LSBs as a balanced tradeoff between the device mismatch and the implementation area. The test chip is fabricated in a 65-nm CMOS process with 1.8-mm × 1.7-mm area [Figure 9(b)]. The PA demonstrates its peak output power from +21.2 to +21.8 dBm over a wide frequency range from 1.7 to 2.4 GHz. The measured peak PA efficiency achieves 44% without using any ultrathick metal layer in the output transformer. A look-up-table-based DPD is used to compensate for

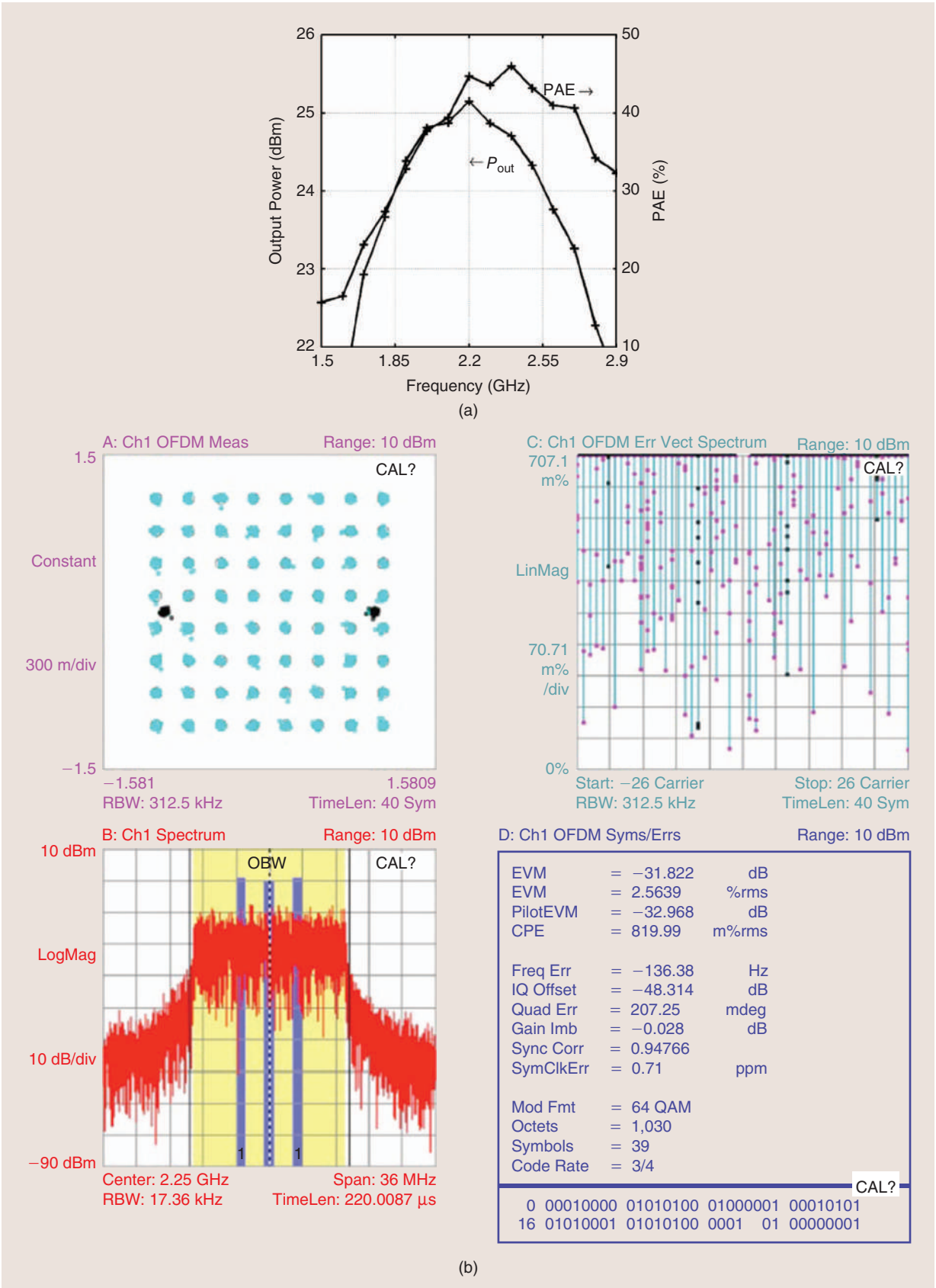

Figure 7. *(a) The measured SCPA output power and PAE versus the carrier frequency. (b) The measured 802.11g 64-QAM signal at the PA output with the demodulated constellation plot (upper left), the OFDM error vector spectrum (upper right), the PA output spectrum (lower left), and the OFDM demodulation measurement summary (lower right).*

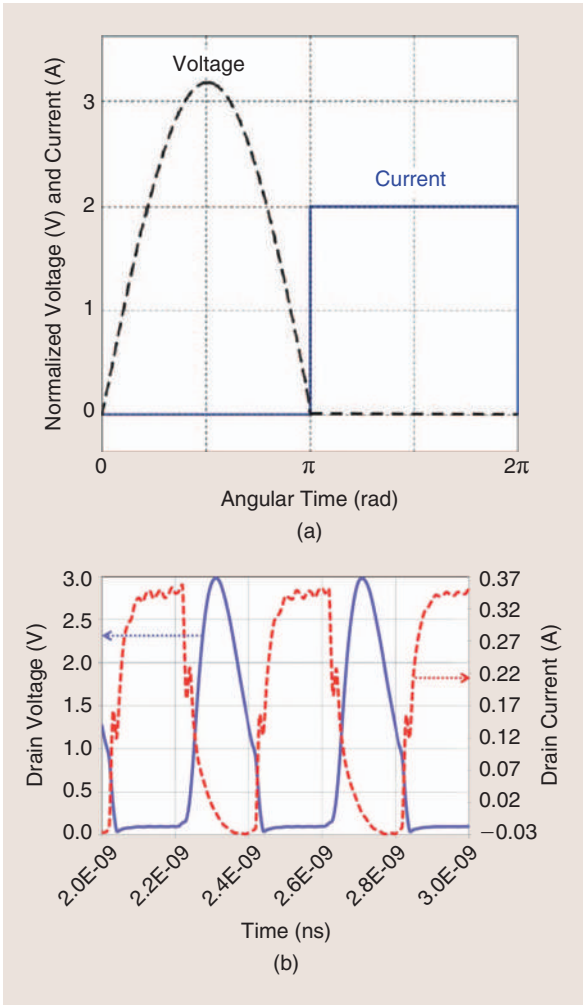

Figure 8. *The transient drain voltage and current waveforms for the class-D^{-1} PA with (a) theoretical waveforms and (b) simulated waveforms.*

the AM–AM and AM–PM nonlinearity of the PA. The PA achieves a good EVM of –28 dB for the IEEE 802.11g 64-QAM OFDM signal at a +14 dBm output power and a 18% PA efficiency (Figure 10). In addition, a low output noise floor of –118 dBm/Hz at 200 MHz offset is also achieved in measurements.

Another design for a class-D^{-1} transmitter with on-chip phase modulator and dynamic load impedance modulation is presented later in [30]. In this design, two identical class-D^{-1} PAs are combined using transformer-based series power combining. Efficiency boosting in the low-power range is achieved by actively modulating the PA load impedance [Figure 11(a)–(c)]. At the −6-dB power back-off, the load impedance for one of the PAs (PA1) can be approximately doubled if the other PA (PA2) is turned off with its differential output nodes shorted [Figure 11(d)]. As a result, this operation sets the load of the PA1 back to its optimum load impedance at this −6-dB back-off power, and the overall PA efficiency is thus almost doubled at this back-off level.

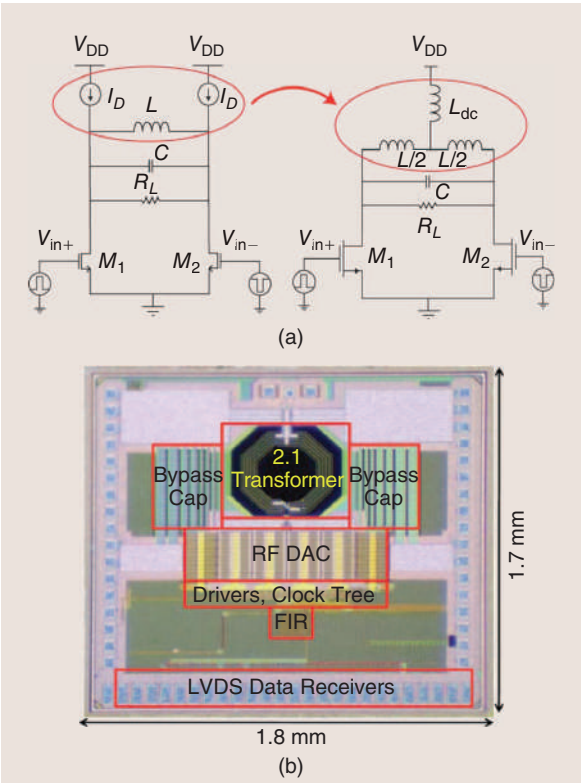

Figure 9. *(a) The practical implementation of the class-D^{-1} PA and (b) a microphotograph of a chip. LVDS: low-voltage differential signaling.*

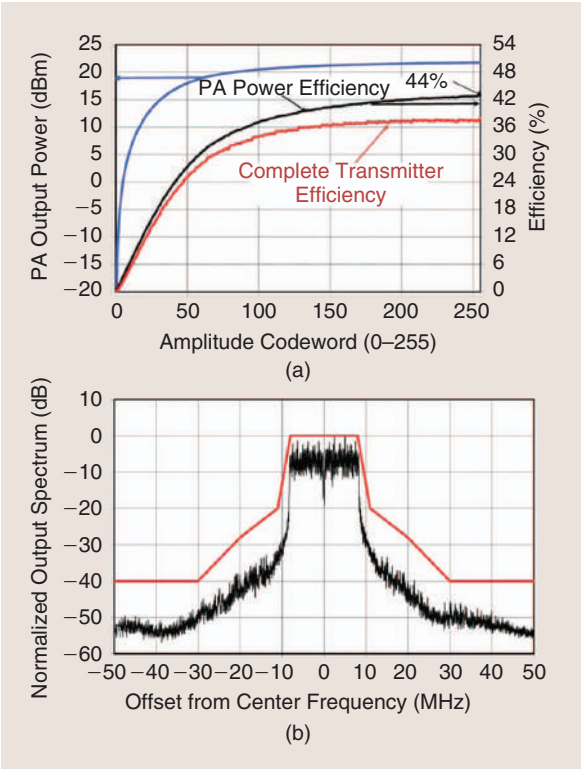

Figure 10. *The class-D-1 PA's (a) output power and efficiency dependence on control code word and (b) output spectrum for an IEEE 802.11g 64-QAM OFDM signal.*

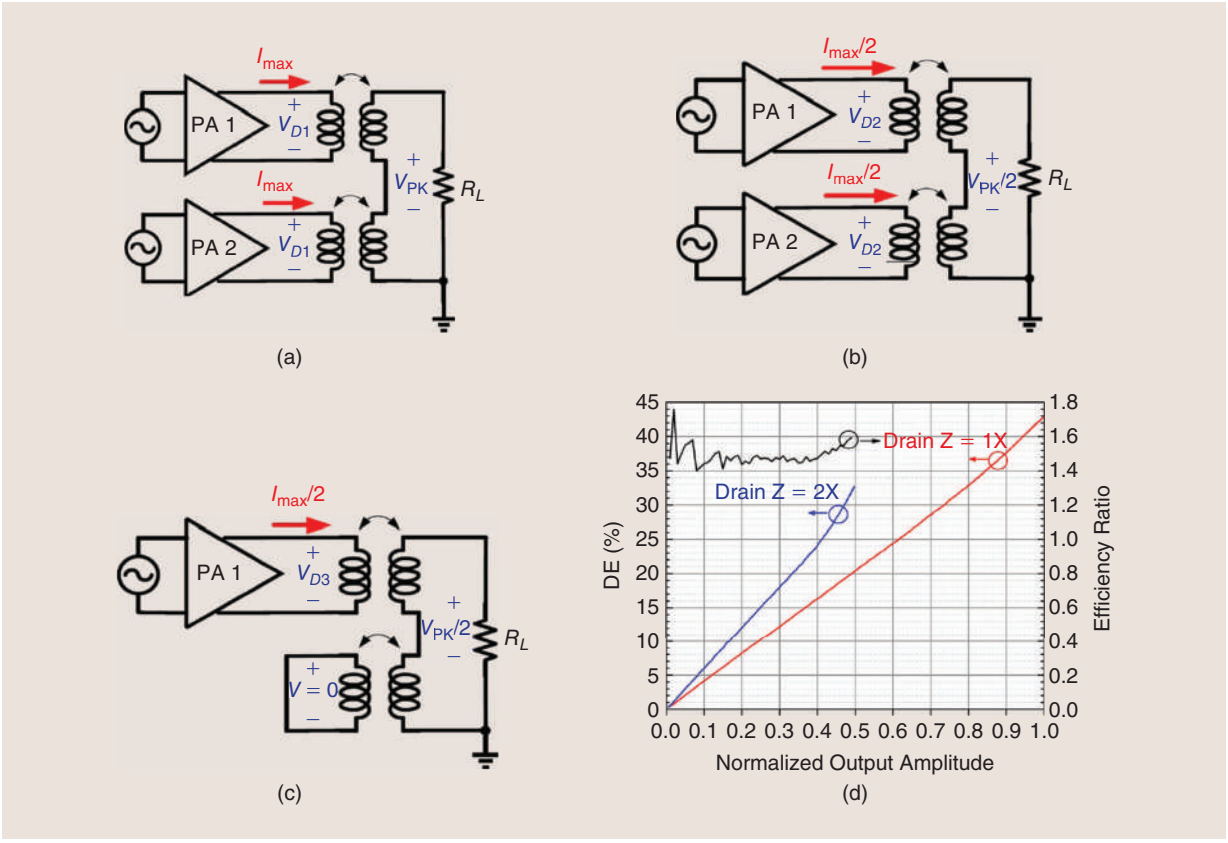

Figure 11. *A class-D-1 PA design with on-chip phase modulator and dynamic load impedance modulation. (a)–(c) Low-/high-power mode switching for PA back-off efficiency boosting at the −6-dB power back-off level. (d) The measured PA DE enhancement during the power back-off [30].*

In terms of the implementation, there are two options to electrically short the output nodes of the turned-off PA (PA2). First, one may introduce a shunt transistor switch at the PA2 output, which should withstand a high RF voltage swing when PA2 is in operation [31]. However, this approach may cause extra delay and efficiency degradation. The second option is to utilize the power transistors in PA2 to short its own output nodes to ac ground, which is implemented in this design [30]. With this dynamic impedance modulation technique, a high DE of 24.5% is achieved for an IEEE 802.11g 64-QAM OFDM signal with –28-dB EVM.

Employing Digital/Analog Techniques to Augment Classic PA Architectures

Class-G PA with Supply Path Switching Technology for Static Power Control and Dynamic Envelope Tracking

Supply voltage modulation such as envelope tracking (ET) is a widely used PA technique to save dc power dissipation at back-off power levels and improve back-off efficiency [18]. However, conventional analog supply modulator designs often encounter tradeoffs across speed, accuracy, efficiency, power handling, and area, which can be challenging for CMOS PA implementations when meeting stringent modern wireless standards. The class-G PA architecture addresses some of these issues by exploiting multiple discrete-level supply voltages selected in an open-loop fashion, instead of performing the traditional analog feedback-based supply modulation [28]. Therefore, a class-G supply controller simply selects the appropriate supply voltage for the specific power level either as a static power control scheme or as a dynamic supply switching for discrete ET. However, the class-G architecture may still require bulky dc–dc converters to generate multiple supply levels in practice.

To overcome the drawbacks, a supply path switching technique is proposed that reconfigures the connections of multiple PA cores between the supply and ground [32]. A direct implementation of this technique divides the original PA into two half-sized PA cores. The supply path is controlled so that the two PAs are either connected in parallel with the supply V_{DD} (state I) in the high-power operation or stacked in series between the supply V_{DD} and the ground (state II) in the power back-off mode (Figure 12). In other words, the full-supply voltage V_{DD} is applied to both PA cores in the high-power mode (state I), and only half supply voltage $V_{DD}/2$ is applied in the

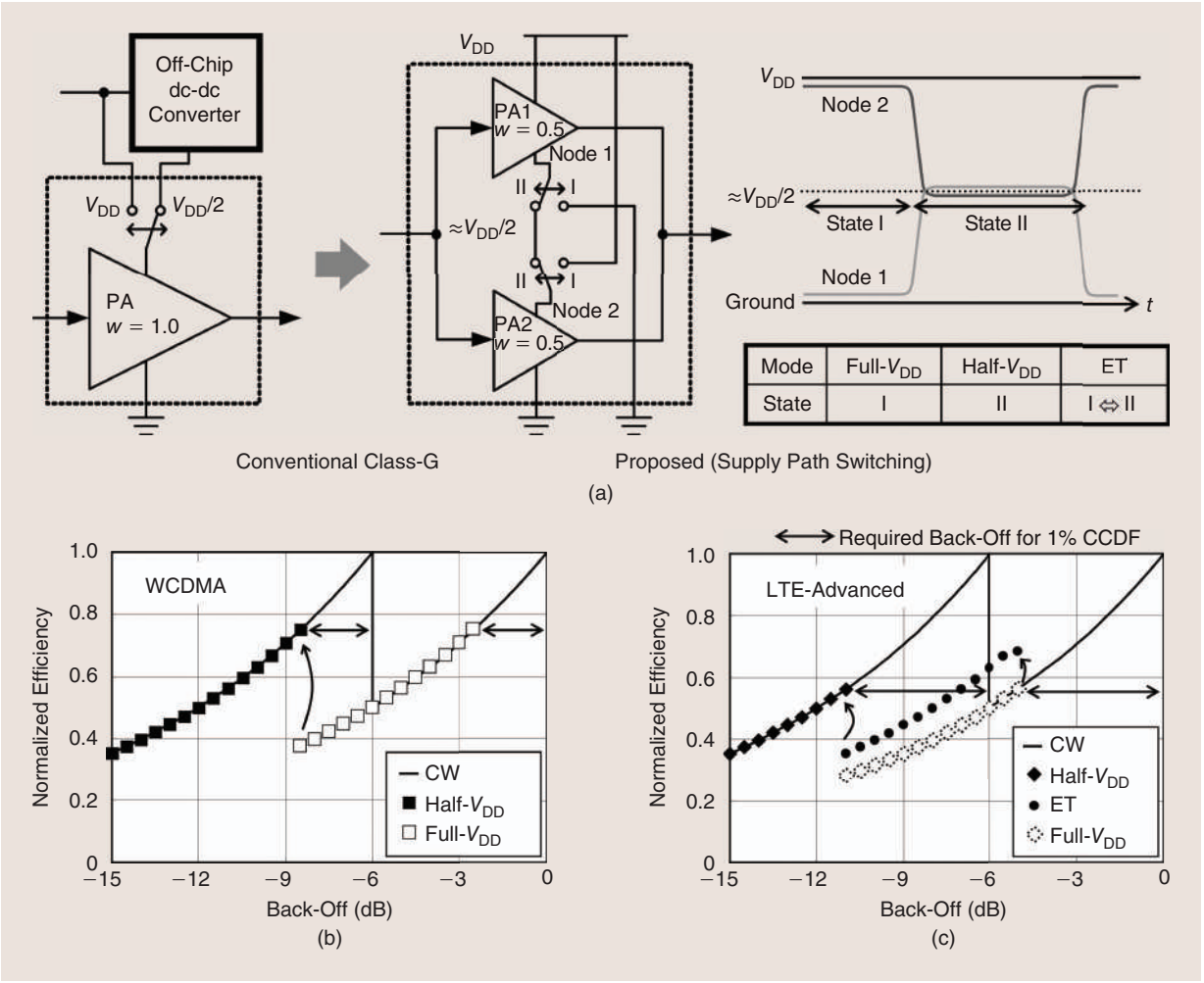

Figure 12. *(a) Conventional class-G supply modulation versus a proposed class-G supply path switching technique. The theoretical efficiency curves for (b) WCDMA and (c) LTE-Advanced signals are also shown. CW: continuous wave; CCDF: complementary cumulative distribution function.*

back-off mode (state II). The input RF driving signal is equally divided and fed into the two PAs, and the two outputs are combined again. The optimal transition point of the supply path is at a −6-dB power back-off assuming a constant PA load impedance and an ideal linear response of the PA. At the −6-dB back-off point, the PA drain voltage swing is half the peak value with a V_{DD} supply. Therefore, by reconnecting the two PA cores in series, the effective supply voltage can be decreased by half, and the resulting power efficiency is doubled.

This supply path switching technique can boost the power efficiency in the back-off range to provide the static transmitter power control required by many cellular standards. Moreover, the supply path switching can be controlled dynamically based on the real-time envelope modulation, and it essentially performs a 1-bit digital class-G operation without any extra dc-to-dc convertors. This is especially useful when the PA needs to amplify complex modulation signals with large PAPR values.

To implement this supply path switching technique in CMOS, a series combining transformer (SCT) and parallel combining transformer (PCT) are used to split and combine the RF signals (Figure 13). The supply path switches are carefully designed to ensure small "on" resistances and a minimum power loss, while maintaining an adequate switching speed. The switches can be automatically controlled, depending on the envelope detected, by an on-chip coupler placed in parallel with the input transformer power splitter (Figure 13). The total delay of the ET path, including the sensing and filtering, as compared with the reference level and the signal buffering operations, is less than 2 ns in simulation. The supply path switching scheme keeps the output RF path constant to ensure that the unwanted load modulation effect is negligible. However, the supply voltage change may introduce discontinuities on the AM–AM and AM–PM responses of the PA. Proper control of the PA biasing can minimize such discontinuities at the expense of certain efficiency degradation. In addition, other conventional

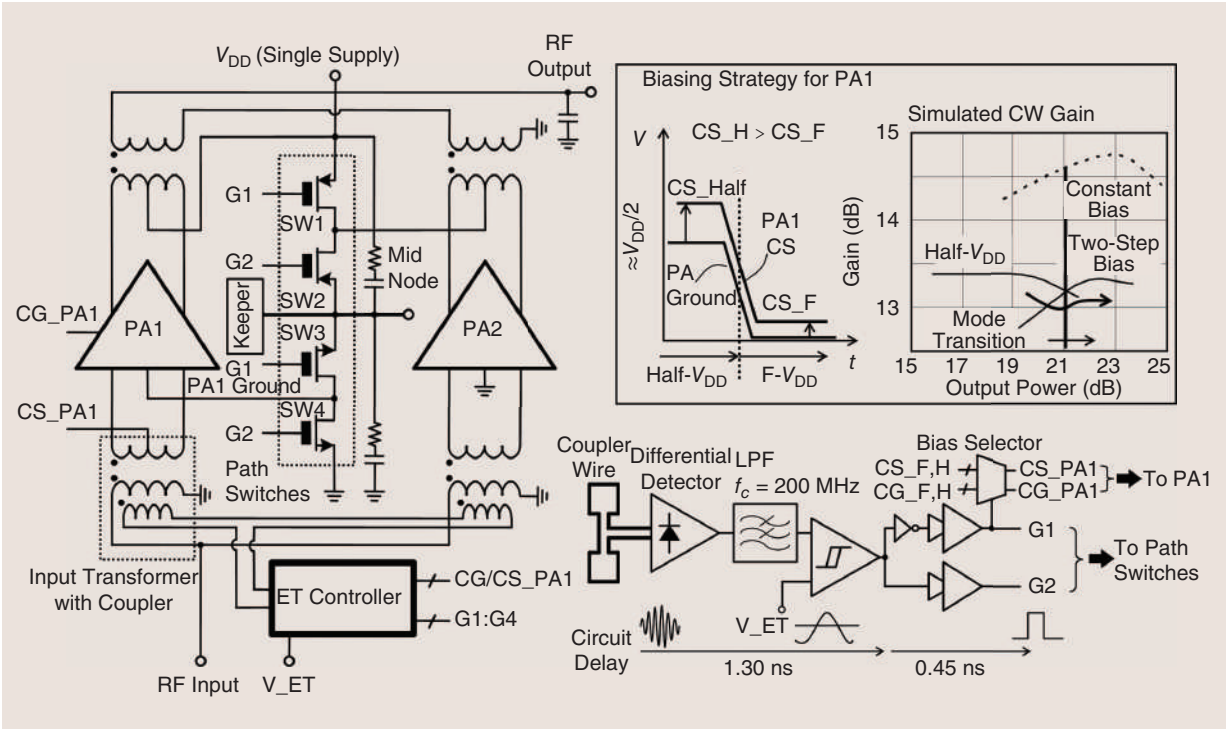

Figure 13. *A transformer-based class-G supply path switching PA implementation in a standard 65-nm CMOS process. The ET controller for bias voltages and supply switches is also shown. CG: common gate; CS: common source.*

nonlinearity compensation techniques, such as analog feedback and/or DPD, can be readily applied to this supply path switching technique for further linearity improvement.

The test chip is fabricated in a 65-nm CMOS process and occupies 2.0 mm × 2.6 mm including the PA cores, input and output transformers, supply path switches, ET controller, and pads [Figure 14(a)]. In the static control mode, the measurement for the 1.8-GHz cellular applications achieves an expected ×2.0 PAE improvement at the −6-dB back-off point for a wideband code-division multiple access (WCDMA) uplink signal and satisfies the −33 dBc adjacent channel leakage ratio (ACLR)-1 specification. For the long-term evolution (LTE)-Advanced signal, both static and dynamic ET modes are tested, and a maximum ×1.35 PAE improvement is measured. A desired 8% rms EVM is achieved for up to a 20-MHz-bandwidth 64-QAM single-carrier frequency-division multiple access uplink signal in the dynamic ET mode [Figure 14(b) and (c)]. Additional analog/digital linearization techniques may further enhance the PA efficiency up to the theoretical ×2.0 improvement at the −6-dB back-off for the dynamic ET mode by reducing the power loss and tightening the linearity margin.

In conclusion, the class-G PA supply path switching scheme utilizes unique analog techniques, i.e., static or dynamic supply switching, to achieve a superior class-G PA operation over conventional implementations for efficiency enhancement in the power back-off mode.

Digital Doherty Polar PA with Digitally Reconfigurable Carrier/Peaking Amplifier Paths

The Doherty PA architecture has been widely used in base stations to enhance PA back-off efficiency [3], [33], [34]. Recently, Doherty PAs with CMOS integration have gained much attention for low-cost mobile applications. Compared with other back-off efficiency enhancing PA architectures, e.g., ET and outphasing, the Doherty PA potentially exhibits a large modulation bandwidth and a moderate implementation overhead. The two-way Doherty PA configuration consists of two amplification paths, i.e., the carrier and peaking PAs [3], [33], [34]. A properly designed Doherty PA ensures that a constant RF voltage swing is maintained at the carrier PA output during the power back-off through the active load modulation between the two PA paths. This results in a substantially improved back-off efficiency, which maintains effective up to a −6-dB power back-off in a classic symmetric two-way Doherty PA [3].

Conventional Doherty PAs are often composed of two analog PAs biased with different conduction angles, e.g., class-AB for the carrier PA and class-C for the peaking PA, so that the power-dependent active load modulation can be realized [Figure 15(a)]. However, such conventional designs typically experience performance degradation due to the imperfect cooperation between the two PAs [3]. Specifically, the peaking PA turning-on point and the relative gain between the two PAs in practice can rarely match the ideal Doherty operation. Although a few analog techniques have been

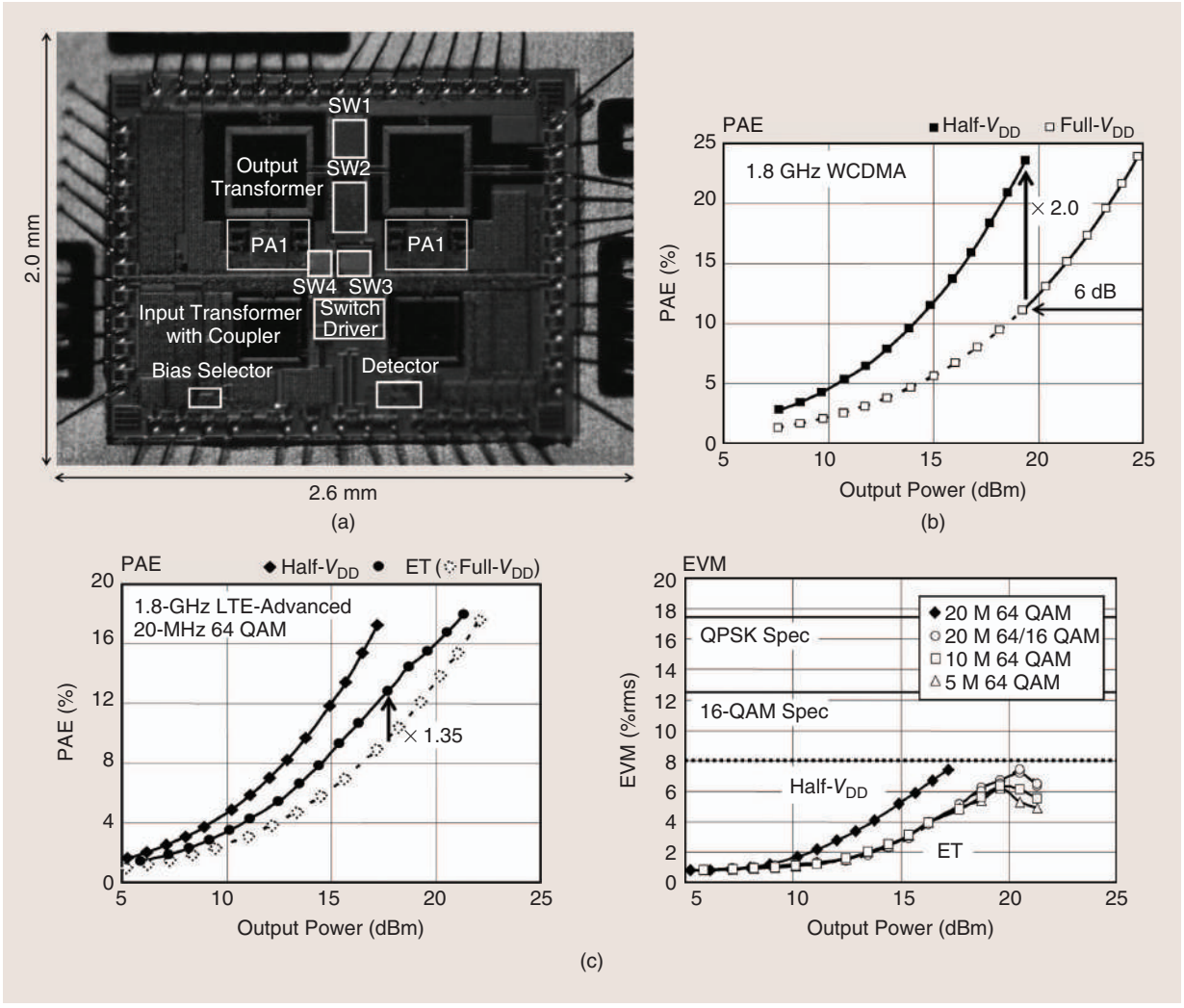

Figure 14. *(a) A microphotograph of a chip for a class-G supply path swhtching PA. (b) The measured PAE for a WCDMA signal achieves ×2 improvement by using the static control mode. (c) The measured PAE for an LTE-Advanced signal achieves ×1.35 improvement by using the dynamic ET control mode while satisfying LTE-Advanced EVM requirements.*

proposed, e.g., dynamic biasing [35], this imperfect two-path cooperation still poses challenges and compromises the Doherty PA's performance in practice. In addition, the bandwidth of a Doherty PA may be limited by the frequency-dependent components, i.e., the input and output $\lambda/4$ transmission lines.

To address these issues, a digital Doherty PA architecture is proposed in which the gains and phases of the two paths can be independently programmed in a digital fashion [Figure 15(b)], [36], [37]. The gain programmability can be realized by implementing the carrier/peaking PAs as two RF power DACs [36]–[38]; and the phase tunability can be achieved by employing varactor loads in the PA drivers [39], whose tuning voltages can be generated using on-chip or off-chip DACs.

The gain/phase programmability makes this digital Doherty PA architecture highly reconfigurable and results in a superior, flexible, and robust Doherty operation. First, the onset point of the peaking PA can be accurately defined, and the relative gain between the two PA paths can be precisely and flexibly set. As a result, the cooperation between the two paths can be optimized, resulting in a superior back-off efficiency in practice over the conventional analog Doherty PAs. This is particularly true when the PA is subject to the antenna impedance variation or process-voltage-temperature (P-V-T) variations since the two amplifier paths can be adjusted in the digital Doherty PA to optimize the Doherty operation [36]. In parallel, the digitally tuned phases of the two paths can be utilized to linearize the PA [39], extend the RF operating bandwidth [39], [40], and compensate the PA load variations [36], [41]. The self-healing/self-compensation capability of the digital Doherty PA architecture against the antenna load variations will be further discussed in the section "Inverse Class-D Digital Polar Doherty PA for Antenna Load Compensation."

The digital Doherty PA architecture is fully integrated in a standard 65-nm bulk CMOS process [Figures 15(c) and 16(a)] [36], [37]. The polar PA topology is adopted. The phase-modulated RF input is first

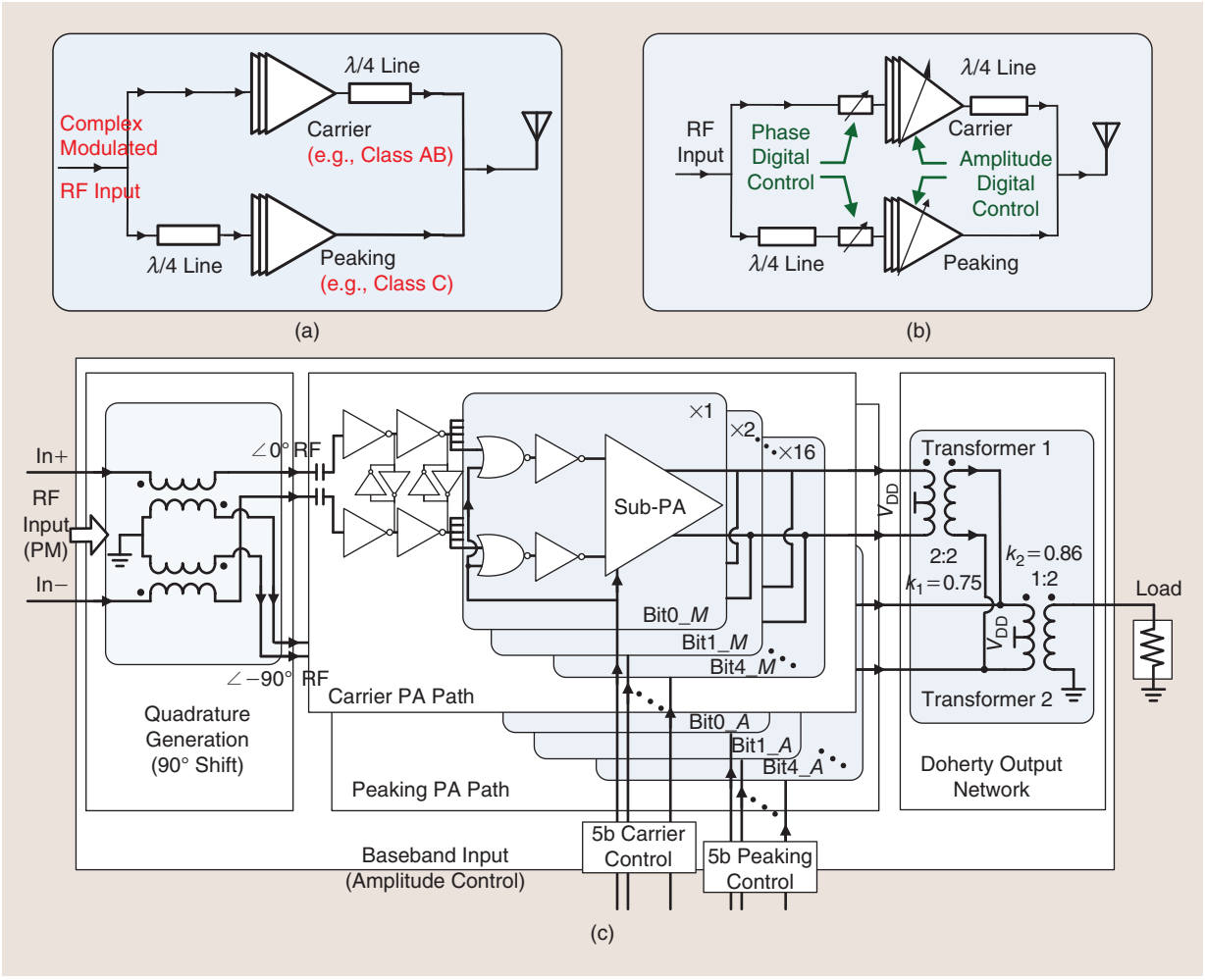

Figure 15. *(a) A conventional analog Doherty PA architecture. (b) A digital polar Doherty PA architecture. (c) A digital polar Doherty PA with carrier/peaking PA gain tunability fully integrated in a 65-nm bulk CMOS process. TM: transformer.*

split into two signals with 90° difference by the input passive network, and the two PM RF inputs are then separately amplified by the two PA paths. The resulting outputs are combined by a PCT-based network, which simultaneously performs Doherty active load modulation, impedance downscaling, power combining, and differential-to-single-ended conversion [36], [37]. The gains of the two amplifier paths can be independently programmed. The digital codes control the two RF power DACs to turn on the proper power cells and real-time synthesize the AM signal. The class-D^{-1} switching PA topology is employed in the power cells for a high peak PA efficiency [29], while the back-off efficiency is enhanced by the Doherty operation.

This PA achieves its peak power of +27.3 dBm at 3.82 GHz. The peak PA DE and PAE are 32.5% and 28.6% at 3.60 GHz, respectively. The maximum absolute and relative efficiency improvement compared with a class-B PA is 7.0% at a −5.4-dB power back-off (from 16.2% DE to 23.2% DE) and 47.9% at a −8.1-dB power back-off (from 11.9% DE to 17.6% DE), respectively [Figure 16(b)]. It achieves 3.5/4.7% rms EVM with +23.5/+22.1 dBm average output power and 26.8/24.1% PA DE for the quadrature phase-shift keying (QPSK) [1 megasymbol/s (MSym/s) and PAPR = 3.7 dB]/16-QAM (500 kilosymbol/s and PAPR = 5.4 dB) signals. The demodulated QPSK measurement result is shown in Figure 16(c).

The digital Doherty PA architecture is further extended in [39]. This design employs a mixed-signal hybrid class-G Doherty PA architecture for PA efficiency enhancement at deep power back-off levels (down to −12 dB), which is far beyond the efficiency enhancement range of a conventional symmetric Doherty PA (−6 dB). Moreover, it utilizes analog techniques to enable independent phase programming of the carrier/peaking amplifier paths. This analog phase assistance and the digital gain tunability achieve a mixed-signal linearization of the PA for high-PAPR signals.

The mixed-signal hybrid class-G Doherty PA architecture operates as follows [Figure 17(a)] [39]. In the first −6-dB power back-off range, the PA utilizes its digital Doherty active load modulation for PA efficiency enhancement. This is also called the "full-V_{DD}" mode, since the PA supply is kept at V_{DD} [see insets 1 and 2

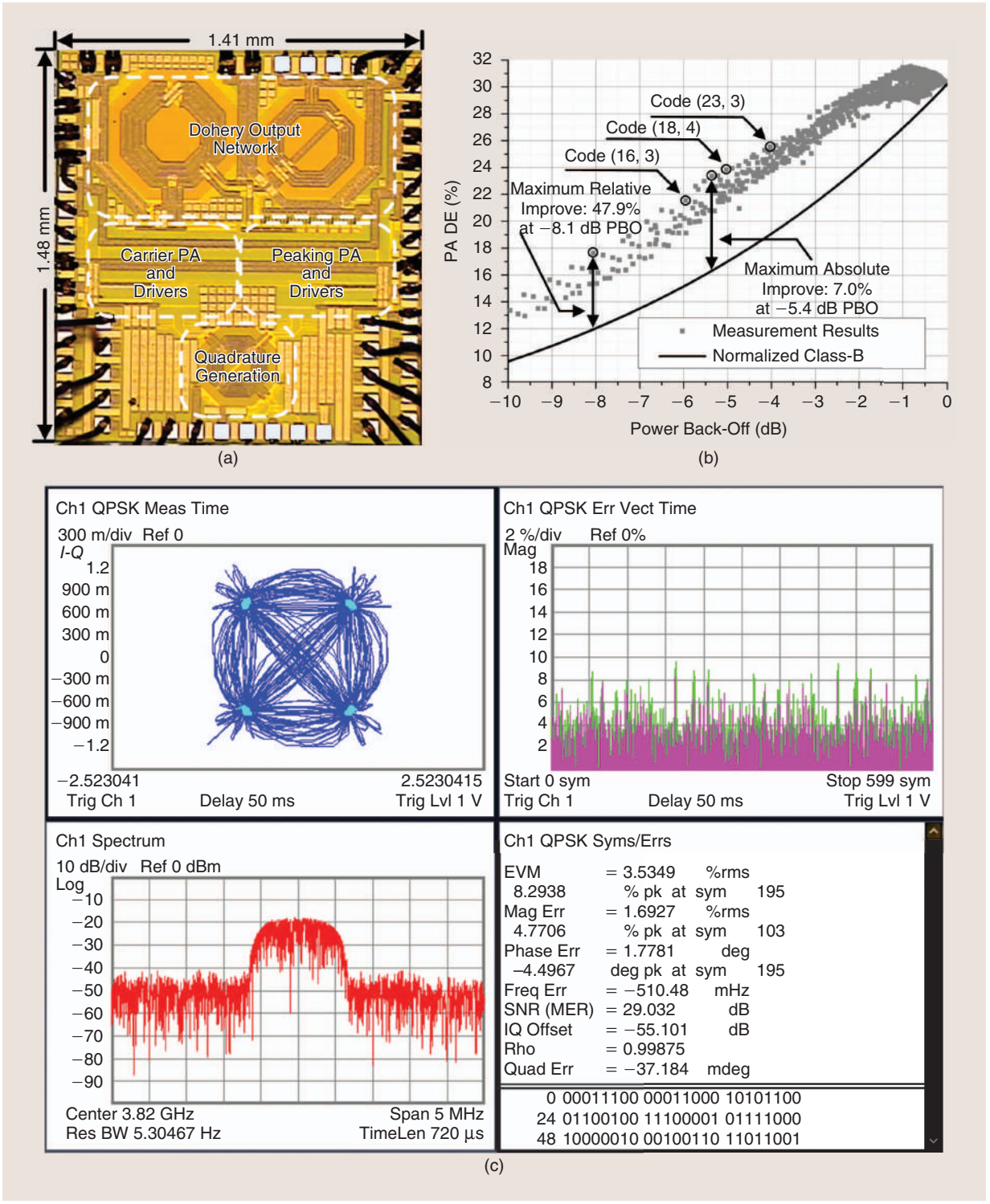

Figure 16. *(a) A microphotograph for the digital Doherty PA. (b) The measured PA DE versus the output power back-off levels. (c) The measurement results with a QPSK modulated signal.*

of Figure 17(a)]. For the power back-off range beyond −6 dB, the class-G digital supply modulator switches the supply to $V_{DD}/2$, and the PA then operates in the "half-V_{DD}" mode [see insets 3 and 4 of Figure 17(a)]. When the PA transits from the full-V_{DD} mode to the half-V_{DD} mode at the −6-dB power back-off point, the RF output currents of the carrier/peaking PA should be digitally reconfigured to half the maximum RF current to maintain the continuity of the output RF power [see insets 2 and 3 of Figure 17(a)]. Note that this current reprogramming also realizes an optimum PA load configuration when the PA enters the half-V_{DD} mode. Thus, the PA can achieve its digital Doherty active load modulation again for the power back-off range of

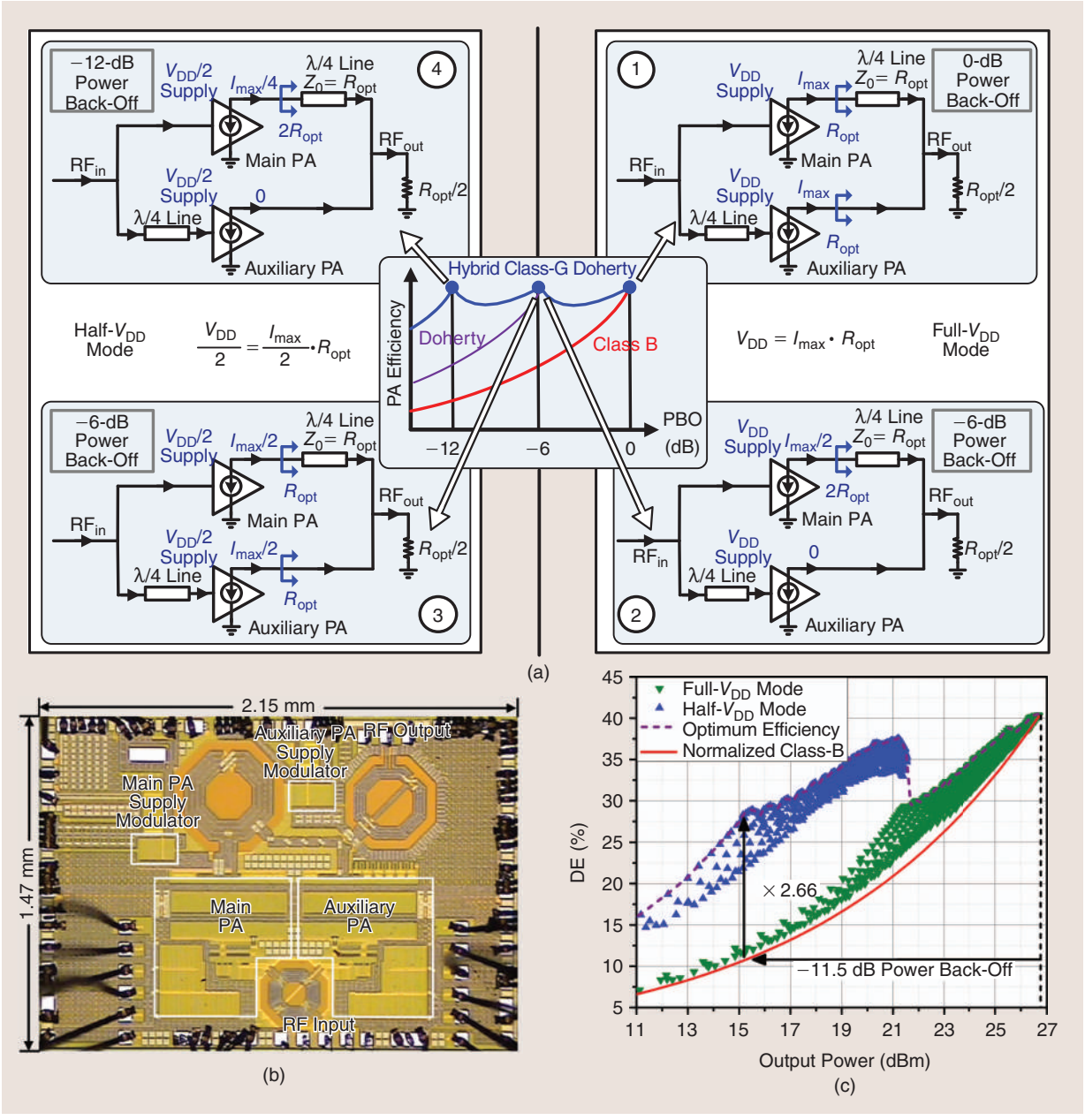

Figure 17. *The mixed-signal hybrid class-G Doherty PA architecture [39]. (a) The operation principal of the hybrid class-G Doherty PA. Inset 1 is the 0-dB power back-off point at the full-V_{DD} mode. Inset 2 is the −6-dB power back-off point at the full-V_{DD} mode. Inset 3 is the −6-dB power back-off point at the half-V_{DD} mode. Inset 4 is the −12-dB power back-off point at the half-V_{DD} mode. (b) A microphotograph of the chip. (c) The measured PA DE versus output power back-off in the continuous-wave test.*

−6 to −12 db. Therefore, only using a 1-bit class-G supply modulator, the hybrid PA architecture substantially extends the Doherty PA operation range from a classic 0 to −6-dB range to a 0 to −12-dB range, which is essential for complex spectrum-efficient modulation schemes.

This mixed-signal hybrid class-G Doherty PA architecture is implemented in a standard 65-nm bulk CMOS process [Figure 17(b)] [39]. At the −11.5-dB back-off, the continuous-wave measurement achieves ×2.66 PA DE improvement over the class-B PA [Figure 17(c)], which is the state-of-the-art back-off efficiency enhancement among reported CMOS PAs without using switches at the PA output. It is further demonstrated that the PA bandwidth can be substantially extended using analog phase tuning to adjust the differential phase between the carrier and peaking PA paths [Figure 18(a) and (b)]. Moreover, the PA AM–PM distortion can be largely compensated for by adjusting the common-mode phase of the two PA paths. As a result, during the modulation test, the mixed-signal hybrid class-G Doherty PA achieves a substantial back-off efficiency enhancement compared with the class-B PA and the single-supply Doherty PA [Figure 18(c)]. The measured EVM (below –20 dB) and ACLR (below –28 dB) for a

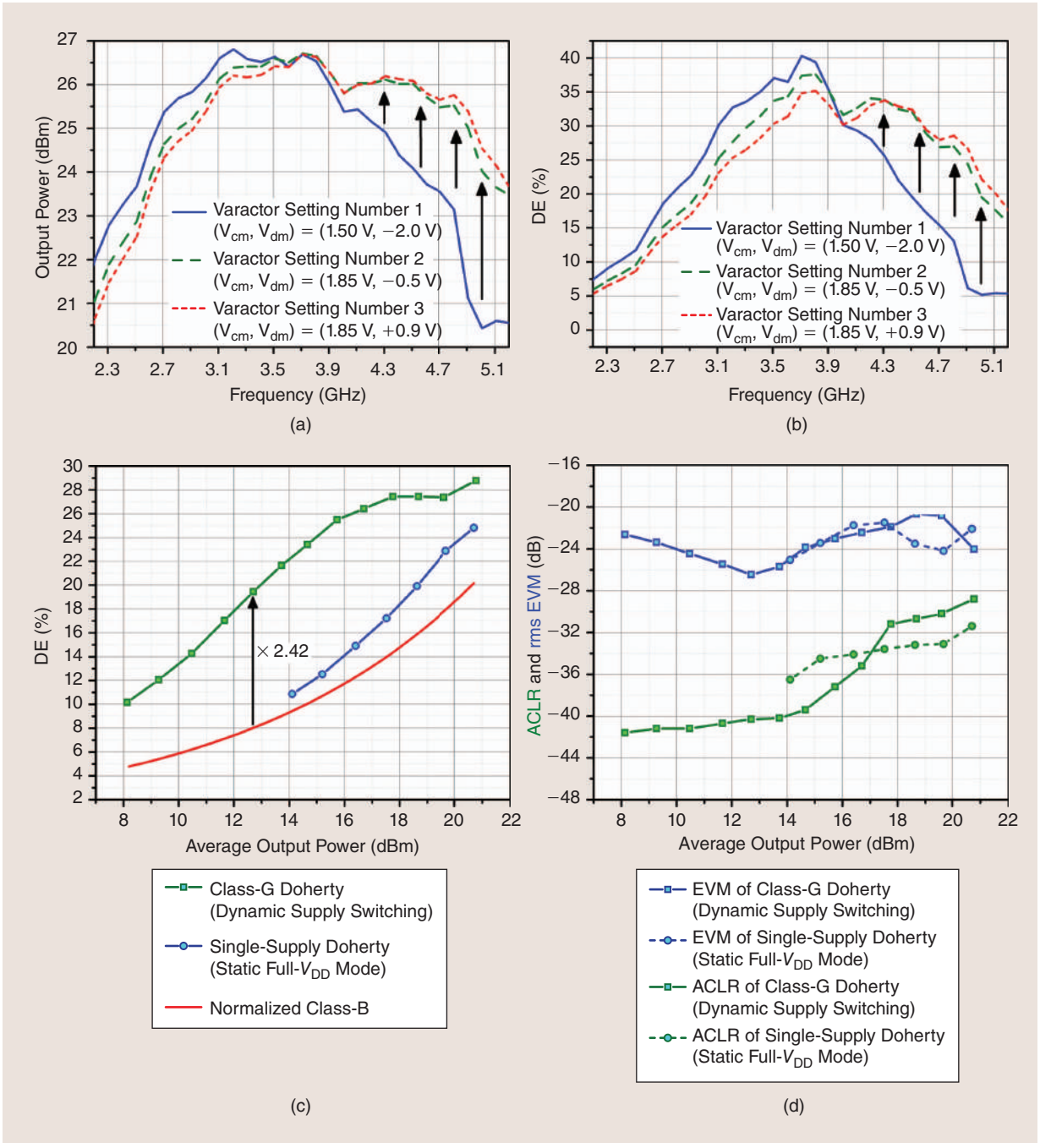

Figure 18. *The measured (a) PA output power and (b) PA DE versus the carrier frequency for the mixed-signal hybrid class-G Doherty mixed-signal PA. The PA bandwidth can be substantially extended by adjusting the differential phase of the carrier/peaking PA paths. The measured (c) PA DE and (d) EVM/ACLR versus averaged output power with a 1-MSym/s 16-QAM modulated signal.*

1-MSym/s 16-QAM modulated signal demonstrate the linearity of the mixed-signal hybrid class-G Doherty PA [Figure 18(d)].

In summary, the digital Doherty PA exploits the use of CMOS digital programing and computation capabilities in a classic PA architecture and substantially enhances the PA's operation, e.g., in terms of efficiency and linearity. In parallel, analog circuit techniques are employed for further PA performance improvement.

Class-D Digital Outphasing PA

The outphasing PA is another popular architecture for PA back-off efficiency enhancement [42]–[44]. The outphasing PA is based on decomposing the complex modulated signal into two constant-amplitude signals $S_1(t)$ and $S_2(t)$, performing separate power amplification, and then combining the amplified signals to restore the modulated signal [Figure 19(a)]. Given a generic complex modulated signal $x(t) = A(t) \cdot \cos[\omega_0 t + \varphi(t)]$, the

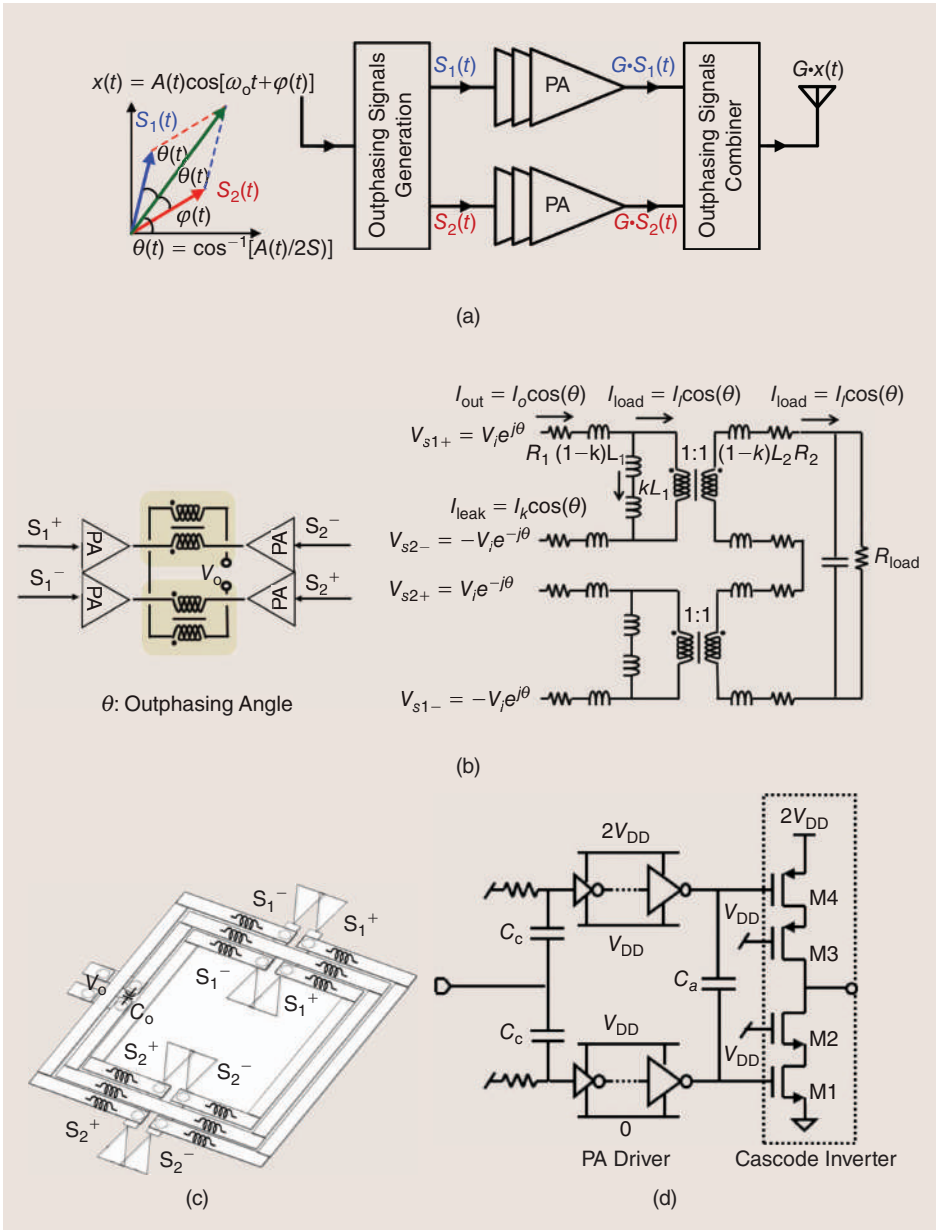

Figure 19. *(a) The outphasing PA architecture. (b) A class-D outphasing PA with a differential transformer-based outphasing power combiner. (c) The layout of the differential transformer-based outphasing power combiner. (d) A class-D cascoded inverter for high output voltage swing ($2V_{DD}$) and high output power. (Figure adapted from [48].)*

two outphasing signals $S_1(t)$ and $S_2(t)$, both with a constant amplitude S, can be expressed as

$$S_1(t) = S \cdot \cos[\omega_0 t + \varphi(t) + \vartheta(t)],$$

and

$$S_2(t) = S \cdot \cos[\omega_0 t + \varphi(t) - \vartheta(t)], \quad (4)$$

where $\vartheta(t)$ is the outphasing angle and $\varphi(t)$ is the PM of the modulated signal $x(t)$ [Figure 19(a)].

The outphasing PA offers unique advantages over other PA architectures with back-off efficiency enhancement. Unlike ET and envelope elimination and restoration (EER) PAs [18], outphasing PAs do not perform polar signal combining and avoid the delay mismatch between the envelope and phase-modulated signals. Compared with Doherty PAs, outphasing PAs can potentially achieve efficiency enhancement for a larger power back-off range. Moreover, the fact that the two outphasing signals both have a constant amplitude enables the use of nonlinear high-efficiency switching PAs and also opens the door to incorporating DPAs [45], [48]. Most importantly, the AM and PM are both carried in the phases of the two outphasing signals $S_1(t)$ and $S_2(t)$. This is particularly suitable for advanced digital CMOS processes, where analog voltages are more prone to distortions, while high-accuracy timing and signal zero-crossings can be readily synthesized and preserved [20].

A major challenge in the outphasing PAs lies in how to achieve the efficient outphasing signal combining at the PA output [Figure 19(a)]. Isolating combiners, e.g., Wilkinson combiners, suffer from PA efficiency degradation at large outphasing angles (small output amplitudes) [3], [46]. Nonisolating combiners lead to coupling and active pulling at the two outphasing outputs, which achieve PA efficiency enhancement but with possible linearity degradations [47].

Recently, a CMOS differential outphasing PA with a transformer-based outphasing combiner and DPA output stages was reported [48] [Figure 19(b) and (c)]. The transformer-based combiner obviates the need for any transmission line or tunable matching element in the outphasing network [42], achieving a substantial design simplification and area saving. Note that a similar transformer-based outphasing combiner has been employed

in an analog outphasing PA [49]. The PA output stages are composed of digital inverter based class-D PAs for constant amplitude amplifications. Class-D PAs are essentially digital inverters; they do not require accurate RF transistor modeling and are fully compatible with digital CMOS processes. However, conventional CMOS inverter-based class-D PAs typically provide output voltage swings lower than the supply voltage V_{DD}. To improve the PA output power capability, particularly for low-voltage scaled CMOS nodes, a cascoded inverter topology can be employed to effectively double the output voltage swing to $2V_{DD}$ [Figure 19(d)].

The reported transformer-based outphasing class-D PA is implemented in a 32-nm CMOS process together with flip-chip packaging [Figure 20(a)] [48]. It achieves its peak output power of +25.3 dBm at a peak total PAE of 35% [Figure 20(b)]. The PA satisfies the wireless local area network standard without additional linearization. The measured 64-QAM 20-MHz-bandwidth Wi-Fi signal at the PA output is shown in Figure 20(c).

To further improve the PA efficiency at deep power back-off levels, multiple outphasing power cells can be implemented together with a transformer-based power combining structure [45]. This PA architecture can be viewed as a hybrid PA architecture with DPAs and outphasing PAs. These DPA power units can be selectively turned on in a dynamic fashion to provide the discrete power levels based on the instantaneous AM signal, while the in-between power levels can be interpolated using the outphasing operations with a high back-off efficiency.

In summary, the class-D digital outphasing PA is another good example that shows how the analog and digital techniques can be utilized together to achieve significant performance improvements in classic PA architectures.

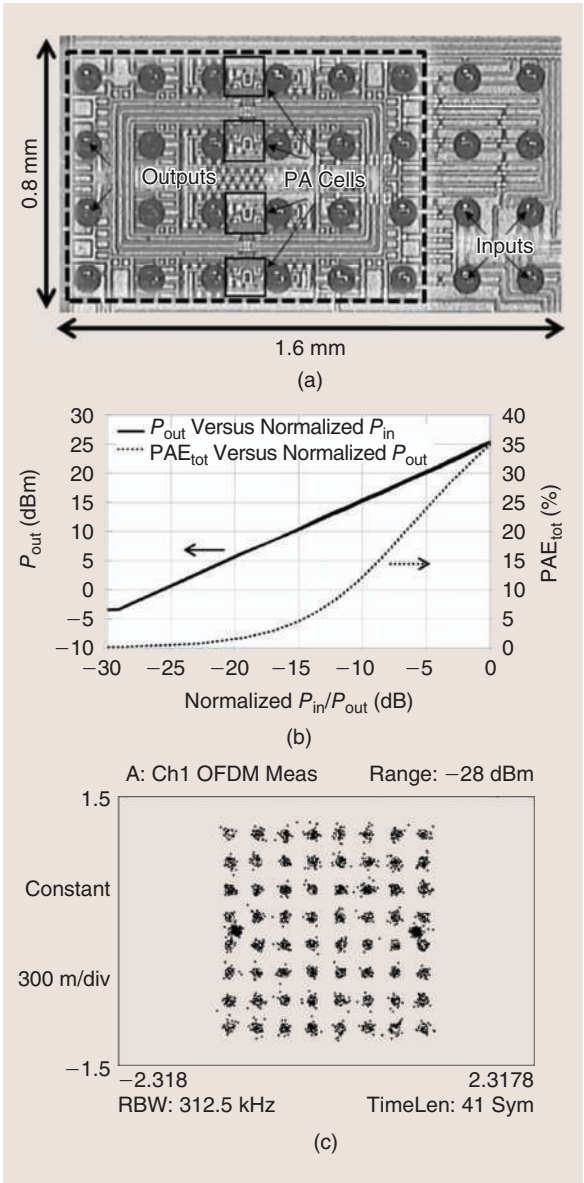

Figure 20. *(a) A microphotograph of the transformer-based outphasing class-D PA in CMOS. (b) The measured P_{out} and PAE versus P_{in}. (c) The measured output 64-QAM constellation at the PA output.*

PA Architecture with Self-Contained Feedback Loop for In Situ PA Linearization

PA Closed-Loop Architecture for In Situ Linearization

As previously described, PAs should perform efficient power amplification while preserving high signal fidelity. Unfortunately, CMOS devices often have inferior

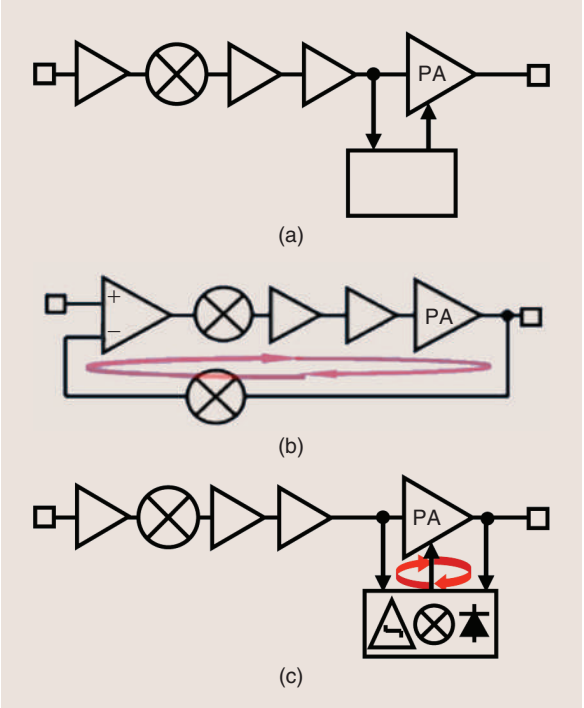

Figure 21. *Conceptual block diagrams of (a) feed-forward, (b) feedback with baseband, and (c) self-contained PA closed-loop feedback for in situ PA linearization.*

The ever-growing demand for higher data rates, power efficiency, and robust operations poses increasingly stringent performance requirements on wireless transceiver systems.

linearity performance compared to III-V HBT devices largely due to their nonlinear device intrinsic capacitances [50]. Therefore, proper linearization techniques are required for viable CMOS PA solutions. Many linearization techniques have been proposed (Figure 21). The DPD [51], [52] is a widely used method, as it is compatible with many PA architectures and is capable of compensating for high-order nonlinearity distortions. However, DPD often requires a global feedback loop from the PA output to the digital baseband to compute and calibrate the distorted symbols. Other conventional analog feedback methods, i.e., Cartesian and polar feedbacks, also require similar global feedback loops for real-time distortion cancellation [53] [Figure 21(b)]. Besides the complexity, the large group-delay in such a global feedback loop inevitably limits the loop bandwidth, posing a challenge in high-data-rate applications. In addition, several feedforward techniques have also been proposed [54] [Figure 21(a)]. Since they rely on nonlinearity cancellation, their efficacy may be compromised under P-V-T and load condition variations.

To address these challenges, a self-contained PA closed-loop feedback architecture utilizing both analog and digital signal processing capabilities in CMOS has been recently reported for in situ PA linearity improvement [55]. An integrated local feedback directly controls the final output stage of a watt-level CMOS PA and overcomes the bandwidth issue typically encountered in global feedback loops [Figure 21(c)]. Therefore, this architecture offers an inherently large bandwidth, since the loop is completely embedded within the PA with a small loop delay. Although a stable feedback loop at the RF frequency can be challenging, a polar feedback architecture with separate phase and amplitude paths can readily mitigate the instability issue.

A detailed conceptual block diagram of the self-contained PA closed-loop feedback architecture is shown in Figure 22. The reference PA is designed to be always linear with a reduced gain and scaled load impedance. The amplitude and phase of the PA output and the reference output are compared to generate the error signals of amplitude (V_A) and phase (V_ϑ). The amplitude is detected by a MOSFET power detector. As for the phase path, the outputs of the reference and the main amplifiers are rectified by the limiting amplifiers to remove the amplitude variations but preserve the phase difference. Then a mixer-base phase detector converts their RF phase difference into a baseband signal. The feedback attenuation ratio ($a < 1$) and the phase offset ϕ are predetermined to compensate for the inherent gain and phase difference between the main and reference amplifiers and ensure that the comparison results, V_A and V_ϑ, are both zero when the main PA is linear. This technique can linearize the PA over a very wide RF frequency range by applying the appropriate gain and phase offsets for different operating frequencies. Finally, the error signals are fed back to the PA to perform the gain and phase linearization.

In practice, this PA closed-loop feedback architecture offers unique advantages over conventional PA linearization designs by suppressing the nonidealities of the amplitude and phase detection/comparison circuits at RF frequency. These RF signal detectors typically exhibit nonidealities, such as AM–PM conversion in the phase detector. In this proposed architecture, because it has symmetric detectors for both main and reference amplifiers, these nonidealities can be largely suppressed as the common-mode distortions, thereby achieving

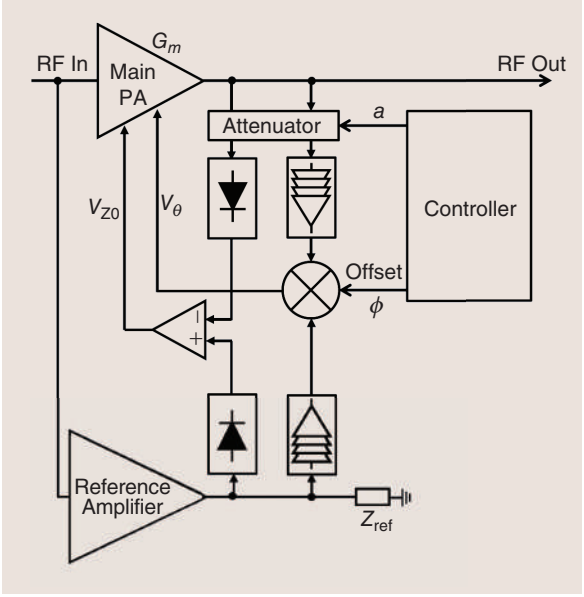

Figure 22. *A block diagram of the self-contained PA closed-loop feedback for in situ PA linearization [55].*

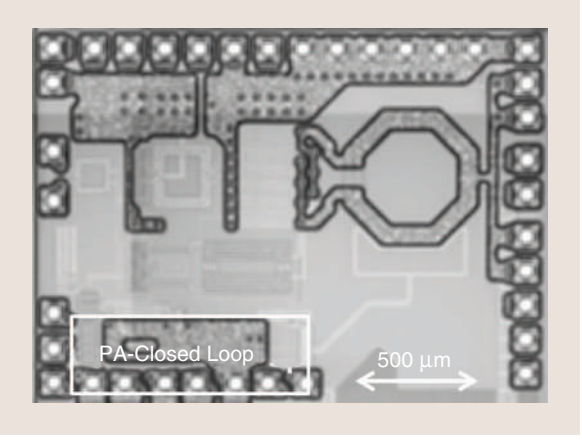

Figure 23. *The die micrograph of the CMOS PA with self-contained PA closed-loop feedback for in situ PA linearization.*

accurate RF signal detection, low power consumption, and a small chip area at the same time. A proof-of-concept design is implemented in a standard 65-nm bulk CMOS process (Figure 23) [55]. The PA closed-loop linearization circuit only consumes an additional 28 mA from a 1.5-V supply and a small chip area overhead (Figure 23). When amplifying a WCDMA compliant signal, the PA closed-loop architecture improves the output power of a CMOS PA from +25.9 dBm to +27.9 dBm, and the total PAE is improved from 30% to 39% (including the power consumption of the linearization circuit).

Therefore, this self-contained in situ PA closed-loop feedback architecture is also a good example that shows how well-arranged analog and digital techniques can be employed to improve the large-signal operation in RF PAs.

Enhancing PA Robustness Against Antenna Load Variations

PA Closed-Loop Architecture with a Silicon-on-Insulator Tuner for In Situ Antenna Impedance Detection and Mismatch Compensation

Due to the recent demands for small-sized antennas, antenna load mismatch is becoming an increasingly important issue [8]–[10]. Automatic impedance detection and mismatch tuning are becoming necessary in mobile or field-deployable wireless transmitters. Several impedance detection techniques have been proposed that measure the antenna mismatches by the magnitude of the antenna load reflection coefficient $|\Gamma\text{Antenna}|$ and minimize this mismatch by controlling an impedance tuner [56]–[58] [Figure 24(a)]. PA reliability improvement is an additional benefit by employing antenna impedance tuning, since it avoids device stressing due to the antenna load mismatch.

Unfortunately, the reported techniques cannot address all the issues in the antenna load mismatches. First of all, most existing antenna load detection techniques only detect the amplitude of the load reflection coefficient without any phase information. Moreover, wide-band PAs [11], [14] may prefer a frequency-dependent optimum load instead of a constant 50 Ω for wideband operations. Furthermore, a typical PA design exhibits a degraded power efficiency with a constant 50-Ω load at the back-off power levels. In addition, the antenna impedance mismatch is actually time dependent due to the antenna proximity effect. Therefore, a desired impedance detection/tuning scheme should promptly and precisely detect the vector impedance with both amplitude and phase information.

The PA self-contained in situ closed-loop architecture can be extended to realize a vector-based antenna load detection [59] [Figure 24(b)]. In the impedance detection mode, a linear reference PA drives a known load scaled from the optimum PA load. Then, the actual load impedance of the main PA (Z_{PA}) can be detected by V_A and V_ϑ, which, respectively, correspond to the amplitude and phase deviation of the actual main PA load from the optimum complex PA load, if both the main and reference PAs are linear. The detected difference will drive the silicon-on-insulator (SOI) tuner to set the main PA load impedance to the optimum value. Again, the feedback attenuation ratio ($a < 1$), phase offset (ϕ), gain of the reference amplifier (G_{m2}), and the reference impedance (Z_{ref}) can be designed and programmed such that the comparison results, V_A and V_ϑ, are both zero when the main PA load matches the optimum complex PA load impedance (Z_{opt}).

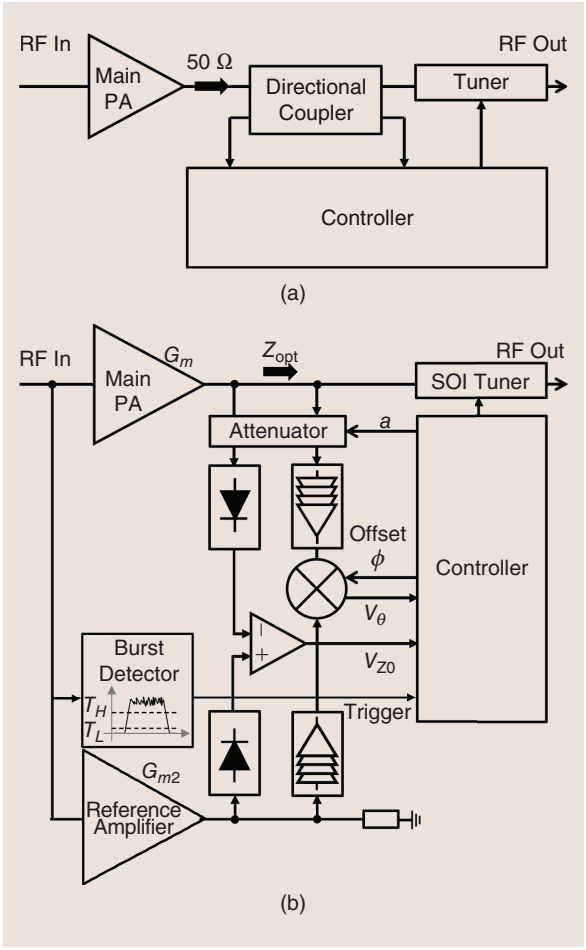

Figure 24. *Antenna load impedance detection and tuning schemes. (a) The conventional approach of detecting the reflection coefficient using a directional coupler. (b) Vector impedance detection by using the PA closed-loop architecture.*

Interestingly, this architecture can also automatically retune the load impedance to its optimum value at reduced output power levels, i.e., during PA power back-off. For example, if the total effective G_m of the main amplifier is lowered in the power back-off, e.g., by reducing the total gate width of the enabled CMOS PA cells in a DPA, the load impedance then can be increased by the same factor through the impedance detection and retuning. Therefore, the PA DE can be restored to its theoretical optimum value based on the load-line

The proposed mixed-signal PAs can be readily extended to a multimode/multistandard wireless transmitter.

theory. In practice, a slight degradation exists due to the non-idealities in the on-chip matching network [59].

To measure the impedance when the main PA is operating linearly, the PA design performs the antenna load detection and calibration during the ramp-up stage [59]. An automatic tuning sequencer is implemented by taking advantage of the CMOS signal processing capability. The closed-loop impedance measurement and adjustment are triggered by an on-chip burst detector that checks the power ramp-up stage of the PA. Two power detectors are implemented with a 15-dB threshold level difference. The sequencer triggers the load tuning only when the input signal amplitude crosses the two thresholds within more than a few microseconds. This automatic tuning sequencer can reliably detect the PA power ramp-up stage without false triggering by the modulated signals and can initiate the autonomous antenna load tuning appropriately.

For the antenna load tuning, a low-loss impedance tuner is realized on an SOI switch die by utilizing recent advances in SOI technology [60]. The loss of the tuner ranges from 0.3 to 3 dB and from 0.3 to 4.6 dB to cover a voltage standing wave ratio (VSWR) circle of 4.5:1 and 6:1, respectively. In the near future, CMOS-based band-selection switches, an impedance tuner, and a CMOS-PA can potentially be integrated on the same chip to further reduce the form factor and packaging complexity. The measured PA performance with WCDMA standard compliant signals under the antenna load variations is shown in Figure 25. The SOI tuner board schematic and tuning performance are shown in Figure 26.

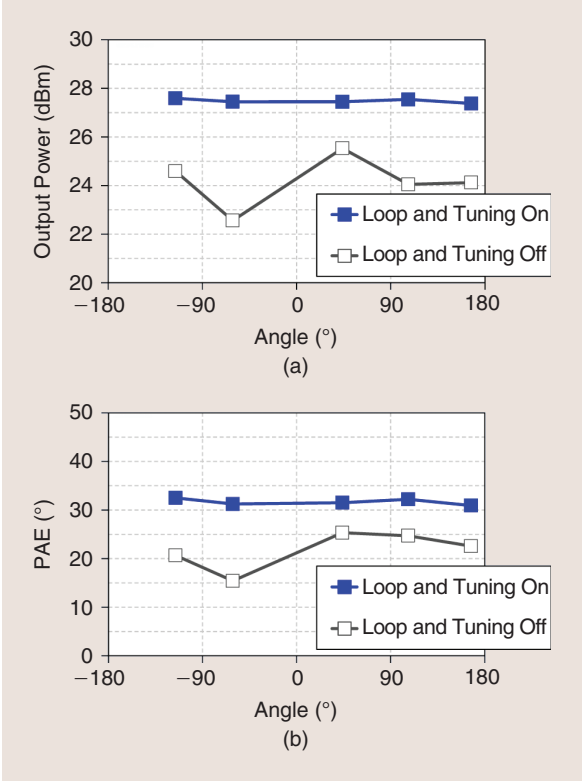

Figure 25. *The measured PA performance with WCDMA standard compliant signals under the antenna load variations. (a) The measured PA output power and (b) PAE under mismatched load of VSWR = 2.5:1 with and without the PA closed-loop based load tuning.*

Inverse Class-D Digital Polar Doherty PA for Antenna Load Compensation

As mentioned in the previous section, a high-quality impedance tuner structure may require dedicated processes, such as SOI or IPD processes, which often are not supported in low-cost standard bulk CMOS processes.

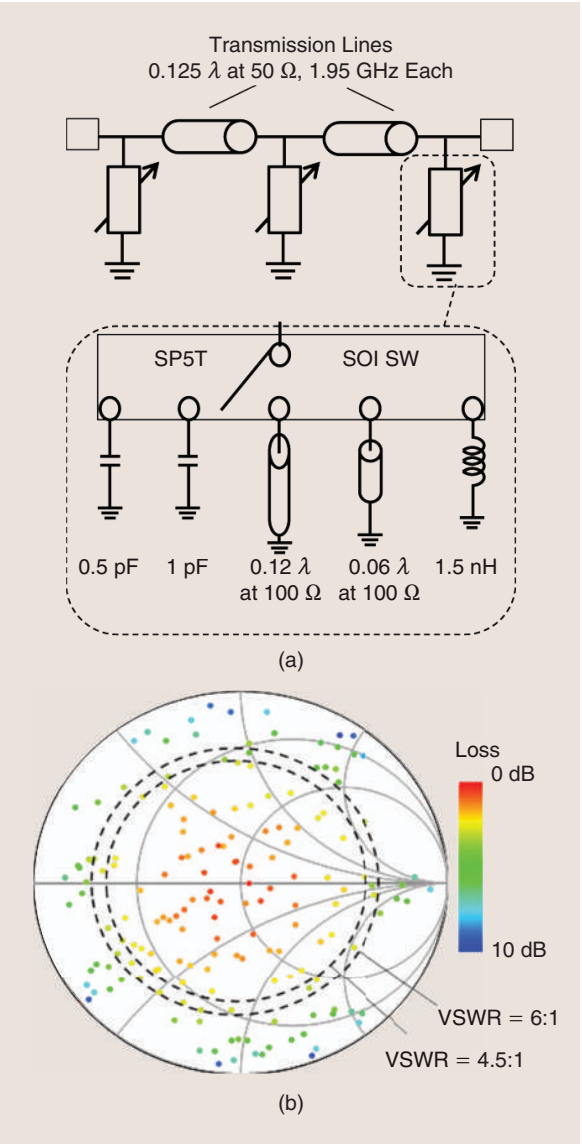

Figure 26. *(a) A schematic of the SOI tuner board and (b) its measurement result.*

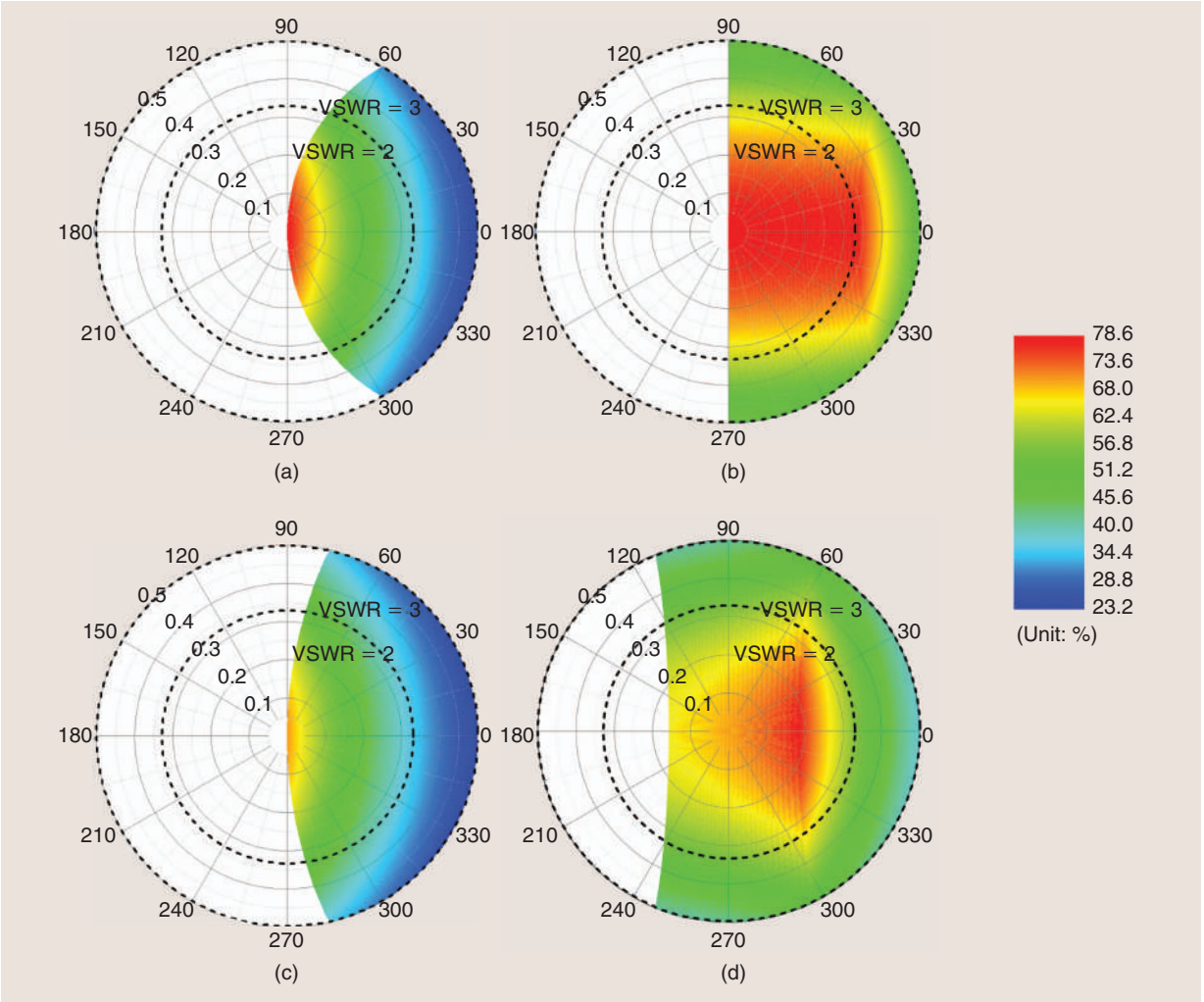

Figure 27. *PA DE for different antenna loads within the VSWR = 3:1 load circle: (a) PA DE for the analog Doherty PA at the peak PA output power, (b) recovered PA DE for the digital Doherty PA at the peak PA output power, (c) PA DE for the analog Doherty PA at the −3-dB PA output power back-off, and (d) recovered PA DE for the digital Doherty PA at the −3-dB PA output power back-off. (a)–(d) share the same color bar. Due to the class-B PA operation assumption, the efficiency at the matched load is 78.5% for the peak PA output power and 70.2% for the −3-dB power back-off.*

As an alternative antenna load tuning approach, it has recently been reported that the digital Doherty PA architecture can achieve PA performance restoration under antenna load mismatches and demonstrate effective antenna load compensation [36], [37], [41]. This is because a digital Doherty PA architecture supports independent and flexible gain/phase programming of the two Doherty amplifier paths with 90° phase difference, which can together reconfigure the Doherty active load modulation and effectively compensate for the antenna load variation.

Figure 27 shows the theoretical study of this Doherty-based load compensation effect within VSWR = 3:1 antenna load mismatches at 0- and −3-dB power back-off levels [41]. In this theoretical study, the carrier and peaking amplifiers are assumed to be class-B analog PAs or 5-bit binary-weighted DPAs, both with zero knee voltages, tuned-out device parasitics at the fundamental frequency, and harmonic-short terminations. The Doherty output network is assumed to be lossless for simplicity, but the passive loss can be readily included [41]. Figure 27(a) and (c) shows the PA DE values of a classic analog Doherty PA at peak output power and the −3-dB power back-off without any gain and phase tuning capabilities under VSWR = 3:1 impedance variations. Figure 27(b) and (d) shows the PA DE results for the digital Doherty PA at peak output power and the −3-dB power back-off with both gain and phase tunability for the effective antenna load mismatch compensations, respectively.

The blank spaces in the plots represent the load regions with RF voltage clipping at the PA outputs and thus potential PA reliability issues. However, the clipping regions are always smaller for the digital Doherty PA compared with the analog Doherty PA at the same power back-off level. This shows that the digital Doherty PA achieves the enhanced linearity and improved reliability performance under mismatched antenna loads. In addition, the digital Doherty PA also achieves an

improved PA efficiency. For example, for both the analog and digital Doherty PAs with matched loads, the efficiencies at 0-dB power back-off are 78.5% assuming the class-B PA operation. When a load mismatch of VSWR = 3:1 and phase(Γ) = 0° is presented, the PA efficiency at the 0-dB power back-off degrades to 26.2% for the analog Doherty PA [Figure 27(a)], which can be recovered to 46.5% in the digital Doherty PA by amplitude/phase reprogramming [Figure 27(b)]. The relative gain and phase of the two PA paths in the digital Doherty PA

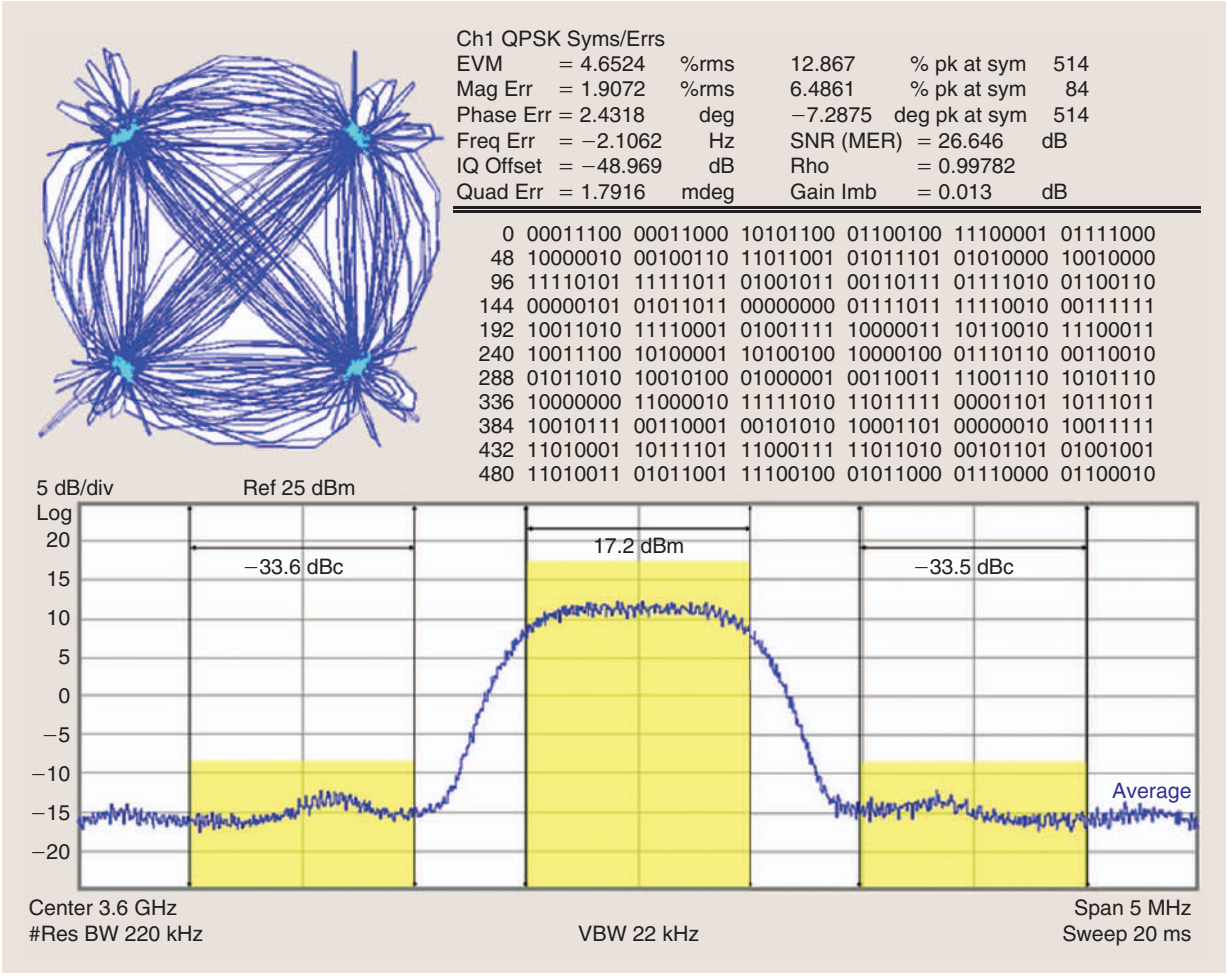

Figure 28. *The measured EVM and ACLR of a digital Doherty PA with a mismatched load (VSWR = 2:1 and phase (Γ) = +60°) at 3.6 GHz after optimizing the gain and phase of the carrier/peaking amplifiers. A 25% PA relative DE enhancement over the class-B PA is achieved in this case.*

TABLE 2. Measured efficiency and linearity with mismatched loads using different digital Doherty code sets for a QPSK modulated signal (1 MSym/s).

Load and Code Set		Absolute η Improvement (%)	Relative η Improvement (%)	EVM (%)	ACLR (dBc)
VSWR = 2:1	EOCS	2.3	15	4.95	−31.7
Phase (Γ) = 0°	DCS	1.3	8	4.78	−34.0
VSWR = 2:1	EOCS	3.5	25	4.65	−33.5
Phase (Γ) = +60°	DCS	2.4	16	4.45	−35.6
VSWR = 2:1	EOCS	3.4	22	4.79	−30.3
Phase (Γ) = −60°	DCS	3.0	20	3.94	−32.3

For a given antenna mismatch, the efficiency optimum code set (EOCS) stands for the digital Doherty PA amplitude interpolation codes for optimum PA efficiency, while the default code set (DCS) is the default amplitude codes for a standard 50-Ω load (without considering the antenna mismatch in the presence).

TABLE 3. Measured efficiency and linearity with mismatched loads using different digital Doherty code sets for a 16-QAM modulated signal (0.5 MSym/s).

Load and Code Set		Absolute η Improvement (%)	Relative η Improvement (%)	EVM (%)	ACLR (dBc)
VSWR = 2:1	EOCS	3.7	30	5.34	−34.6
Phase (Γ) = 0°	DCS	2.4	17	4.33	−34.6
VSWR = 2:1	EOCS	4.4	36	5.09	−36.0
Phase (Γ) = +60°	DCS	3.0	22	3.68	−36.2
VSWR = 2:1	EOCS	4.1	34	4.93	−33.8
Phase (Γ) = −60°	DCS	3.4	29	4.75	−34.7

should be properly set to achieve the enhanced efficiency and improved linearity under the antenna load mismatches. Comprehensive analyses in [41] show that the gain tunability is important for efficiency recovery in the digital Doherty PA, while the phase tunability is essential for linearity enhancement when the mismatched antenna load has a substantial reactive part.

This concept has been verified by measuring the digital Doherty PA implemented in a standard 65-nm CMOS process (see the section "Digital Doherty Polar PA with Digitally Reconfigurable Carrier/Peaking Amplifier Paths") subjected to different antenna loads [36], [41]. The measurement results with modulation signals and antenna load mismatches are demonstrated in Figure 28 and summarized in Tables 2 and 3 [41]. These results show that by leveraging the gain tunability in the digital Doherty PA architecture, a significant efficiency recovery can be achieved only with marginal linearity degradation when the antenna impedance variation is present. Although the symmetric digital Doherty PA architecture cannot compensate for the load mismatches in the clipping regions (Figure 27), this can be readily addressed by adopting asymmetric digital Doherty PA designs or employing PA power back-off [41]. In addition, the digital Doherty architecture can be combined with the traditional impedance tuning networks, e.g., an SOI tuner [59], [60], so that the required impedance tuning region of the tuning networks can be substantially reduced.

Therefore, this digital Doherty PA demonstrates that reprogramming the gain/phase of the two parallel amplifier paths in a Doherty PA can effectively compensate for antenna load mismatches without using any impedance tuner structure. Again, this design is also an excellent demonstration of how digital reconfiguration and back-end computation can be leveraged to improve large-signal PA performance at RF frequency.

Summary

In conclusion, the high integration level and unparalleled computation power in CMOS processes naturally allow the design and realization of sophisticated mixed-mode circuits and systems with both analog and digital operations. Exploiting these mixed-mode circuit techniques and codesigning them in conjunction with the RF PAs may augment large-signal, high-power RF operations and enable substantial performance improvements for PA efficiency and linearity. By leveraging these unique advantages of CMOS processes, such "mixed-signal" PAs also present a new paradigm-shift design methodology that may open the door to next-generation CMOS PA solutions.

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