

Active Harmonic Load–Pull for On-Wafer Out-of-Band Device Linearity Optimization

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Abstract—In this paper, we present an active harmonic load–pull system especially developed for the on-wafer linearity characterization/optimization of active devices with wideband modulated signals using the out-of-band linearization technique. Our setup provides independent control of the impedances at the baseband, fundamental, and second-harmonic frequencies presented to the input and output of the device under test. Furthermore, to enable realistic test conditions with wideband-modulated signals, the electrical delays in the load–pull system are kept as small as possible by implementing a novel loop architecture with in-phase quadrature modulators. We have achieved a phase variation of the reflection coefficient of only 5° /MHz for both the fundamental and second-harmonic frequencies.

We demonstrate the high potential of the system for the on-wafer evaluation of new technology generations by applying out-of-band linearization to heterojunction bipolar transistor (HBT) and laterally diffused metal–oxide–semiconductor (LDMOS) devices. For the HBT, we outline a game plan to obtain the optimum efficiency–linearity tradeoff. Finally, a record-high efficiency–linearity tradeoff was achieved (without digital predistortion) for an inverse class-AB operated Philips Gen 6 LDMOS device, yielding 44% efficiency at an adjacent channel power level of -45 dBc at 2.14 GHz for an IS-95 signal.

Index Terms—Device characterization, heterojunction bipolar transistor (HBT), large-signal characterization, laterally diffused metal–oxide–semiconductor (LDMOS), linearity, load–pull, nonlinear distortion, on-wafer, out-of-band linearization.

I. INTRODUCTION

THE GENERAL demand for higher data rates and larger numbers of users within confined frequency bands has led to an increased use of spread-spectrum-based modulation techniques in mobile communication systems. These techniques (e.g., W-CDMA) provide high spectral efficiency at the price of an increased peak-to-average power ratio of the transmitting signal. As a consequence, the transmitting power amplifier must behave linearly over the whole power range, including the

peak power condition, and, at the same time, provide a good efficiency. This classic problem has resulted in an intensive search at the device and circuit level in order to find solutions that provide an improved linearity–efficiency tradeoff.

The traditional way to address this problem is to use Class-AB (all higher harmonics shorted) or inverse Class-AB operation (all higher harmonics open [1]) and simply “back-off” the device from its 1-dB compression point, until an acceptable linearity performance is obtained. Unfortunately, in most practical situations, this yields a rather poor efficiency of the amplifier output stage for signals with high peak-to-average power ratio. To overcome this limitation, recently, linearization techniques have been proposed, which utilize the out-of-band terminations at the baseband and second-harmonic frequencies, to enhance the in-band linearity [2]–[4]. These new techniques can provide excellent linearity up to the compression point of the active device without any compromise in gain or dc power consumption, making it a very valuable option for the realization of efficient, highly linear, low-complexity power amplifiers.

To support the successful implementation of the out-of-band linearization technique and to evaluate device technologies for their linearity, a dedicated large-signal characterization setup is required. To be more specific, such a setup must provide:

- very high dynamic range in terms of signal integrity and measurement range, facilitating the calibrated testing of highly linear devices at all frequencies of interest (e.g., f_0 , $2f_0$, $3f_0$, and third- and fifth-order intermodulation frequency).
- flexible and independent control of the baseband, fundamental, and second-harmonic terminations at both the device-under-test (DUT) input and output over the full Smith chart (e.g., shorts and opens), facilitating optimum terminations for linear device operation.
- A minimized electrical delay in the active loads, to ensure loading conditions versus frequency, as constant as possible, for all frequency components. This is essential to mimic realistic circuit conditions for wideband-modulated signals (e.g., IS-95, WCDMA, and 3GPP).

Unfortunately, current available commercial load–pull systems fail to meet the above-listed requirements. Commercially available passive load–pull systems^{1,2} cannot control the baseband (BB) impedance and do not cover the complete Smith

¹Maury Microwave Corporation. [Online]. Available: <http://www.maurymw.com/>,

²Focus Microwaves. [Online]. Available: <http://www.focus-microwaves.com/>

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chart. The latter problem can be solved with an active load–pull system³ [5], [6]. However, this system contains long electrical delays and thus cannot be used for useful linearity characterization with wideband signals. These facts combined with the high potential of the “out-of-band” linearization technique triggered the development of a custom active harmonic load–pull system.

In this study, we first give the basic principles of the out-of-band matching technique, which yielded the specification of the measurement system. Next, the resulting system configuration is discussed in terms of dynamic range, independent control of the BB, fundamental, and second-harmonic impedances and the minimization of electrical delay in the setup. Based on this, we analyze the practical constraints of the setup for device linearity optimization in terms of power handling, spectral purity, and bandwidth.

In conclusion, the high potential of the out-of-band linearization technique will be demonstrated experimentally, using two-tone as well as realistic wideband-modulated signals, for HBT and laterally diffused metal–oxide–semiconductor (LDMOS) devices of various technology generations.

II. OUT-OF-BAND CANCELLATION TECHNIQUE

In general, large-signal operation of an active device can be modeled by a combination of nonlinear current and charge sources which depend on the voltages of the (internal) device terminals. When driven with a two-tone input signal, the nonlinear sources in the active device will give rise to distortion. For not too large-signal amplitudes, this distortion can be analyzed through the use of Volterra series [7]. In this technique, each of the nonlinear sources is approximated by Taylor series representing the first-, second-, third-, and fourth-order dependency on the nodal voltages. It is common knowledge that the first-order terms determine the desired linear device transfer, while the third-order nonlinearities of the device give rise to third-order intermodulation distortion (IM3), which corrupts the desired signal transfer. These distortion products resulting directly from the third-order nonlinearities are referred to as *direct IM3* products. When applying the *out-of-band linearization technique*, we aim to cancel these *direct IM3* components by making use of the *indirect IM3* products, which are present anyway. These latter distortion products result from the secondary mixing of the fundamental tones with the second-order products (BB and second-harmonic frequencies) over the nonlinear junctions of the device. By controlling the BB and second-harmonic terminations at the input and output of the device, the magnitude and phase of these indirect components can be adjusted. Consequently, the *indirect IM3* components can be used, under some specific conditions, to cancel the direct ones [3]. This method can provide excellent linearity over a large power range up to the compression point [8]. Fig. 1 visualizes the basic principle of the out-of-band linearization technique, which relates to the definition of our measurement setup. The figure shows the typical output spectrum of a nonlinear device driven by a two-tone signal. It must be stressed that the above principles for device linearity apply to any circuit configuration or measurement setup, independently if intentional control of

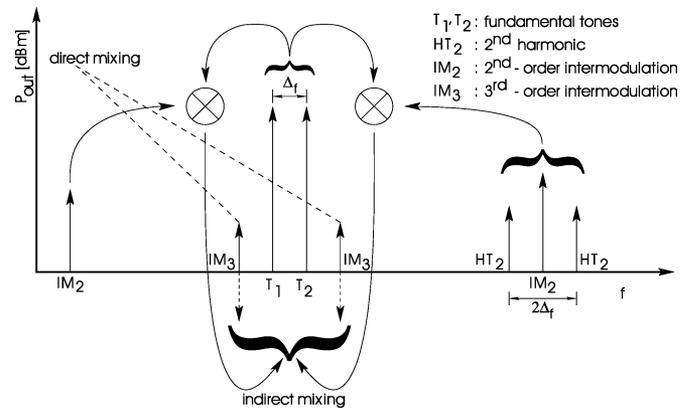


Fig. 1. Basic principle of the out-of-band linearization technique. By controlling the out-of-band impedances at the BB and second-harmonic frequencies, the indirect third-order intermodulation products are used to cancel out the direct ones. The direct components result from third-order nonlinearities, whereas the indirect terms are the consequence of secondary mixing between fundamental and second-order components over the second-order device nonlinearities.

the out-of-band terminations is applied or not. Consequently, to make valid and useful conclusions on device linearity, careful attention must be given to the out-of-band source and load terminations at all times.

In view of the above, independent control of the BB [9], fundamental, and second-harmonic impedances at the input and output of the device is required to optimize the device linearity. In addition, to mimic realistic circuit conditions, the electrical delays of these (harmonic) terminations should be minimized to avoid severe variation of the reflection coefficients within the bandwidth of the modulated signal. These considerations together with the high dynamic range requirement yielded the system definition of our active harmonic load pull system, which will be discussed next.

III. IMPLEMENTATION OF THE ACTIVE HARMONIC LOAD–PULL SETUP

The first attempt to independently control both BB and second-harmonic impedances at the input and output of the device using an active load–pull system was given in [10]. This work was based on loss-compensating duplexers in combination with mechanical tuners to implement the active terminations. Although promising results have been achieved, the system had limitations in the repeatability of the device impedance, measurement speed, and the stability of the active loads when measuring high-performance LDMOS devices. To overcome these problems, in this study, we present a new system that utilizes electronic in-phase quadrature modulators to control the active loads and improved BB impedance control board, supporting fast and extensive device testing and optimization for linearity, as will be demonstrated in Section V. The simplified block diagram of the new setup is given in Fig. 2. The HP 8510 mainframe is used as a linear receiver for both the RF (via the down-converting mixer LO_{HF}) and the BB frequency components (via up-converting mixer LO_{BB}). This avoids the need for a low-frequency oscilloscope to measure the BB signals or impedances. The design of the frequency multiplexer sets the operating frequency of the active loops. Two different

³Progettazione Alta Frequenza. [Online]. Available: <http://www.pafmicro.com>

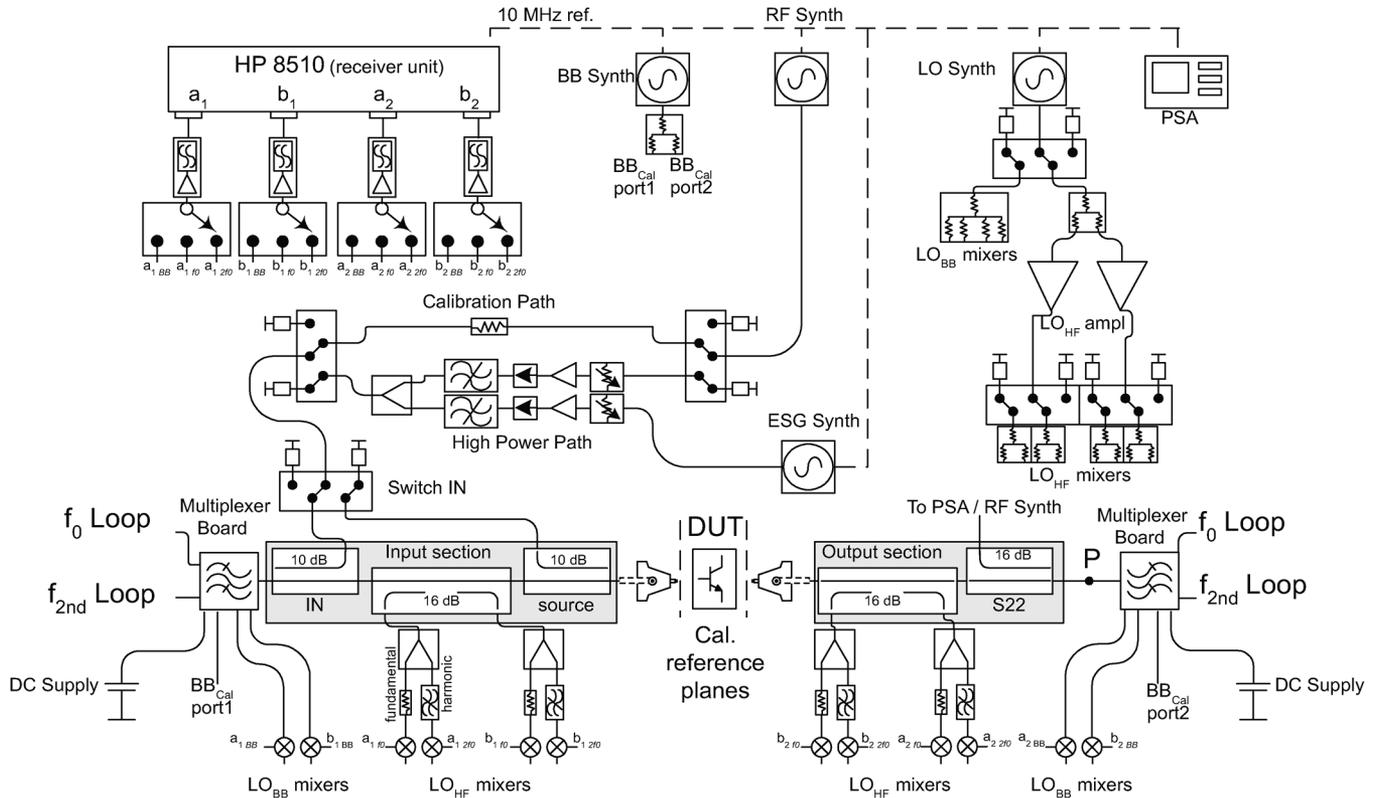


Fig. 2. Block diagram of the active harmonic load–pull system for on-wafer linearity characterization of active devices.

multiplexer frequencies were chosen for the implementation of the active harmonic load–pull system (which we will call the Delft-system hereafter), namely, 1.96/3.92 and 2.14/4.28 GHz ($f_0/2f_0$ harmonic). These frequencies correspond to: Tx. UMTS, Rx. IS95 (1.96 GHz) and Rx. UMTS (WCDMA), and IMT2000 (2.14 GHz). The choice of these bands is based on the high linearity requirements of these communication standards and, consequently, the high interest from industry in optimizing the linearity of power amplifiers intended for these applications. Fixing the fundamental frequency of the loops is required to optimize the system for wideband-modulated signals, as will be discussed in Section IV. The calibration procedure is a combination of the techniques described in [11]–[13] and utilizes the same standards (e.g., short, open, load, and thru) for both RF and BB calibration. This provides a very fast and easy procedure to fully calibrate the system at all frequency components of interest.

A. Dynamic Range

A basic requirement for the characterization of highly linear devices is a spectral clean input signal. In the Delft-system two-tone excitation is achieved by using two independent synthesizers, followed by linear amplifiers, isolators, and low-pass filters. The resulting measured input signal purity yields a third-order input intercept point (IIP₃) of 65.5 dBm, which is more than sufficient for all power amplifier test conditions below a few watts of output power.

To enhance the dynamic range of the HP8510 receiver [14] for the “low” power levels of the harmonic components, at each coupled port of the bidirectional couplers, two mixers are used

to down convert the power waves for detection, namely, a *fundamental* mixer and a *harmonic* mixer. The fundamental tones and intermodulation products (1.7–2.4 GHz) are measured by the fundamental mixer, which provides a maximum dynamic range of 80 dB for the IM3 measurements. All of the higher harmonics are measured by the *harmonic* mixer, which uses a high-pass filter (passband of 3.0–26.5 GHz) in the signal path. This filter provides a rejection of the fundamental signal by 40 dB and therefore eliminates the need for an attenuator in front of the mixer, to avoid the generation of spurious responses by the mixer itself. This maximizes the dynamic range of the system for these signal components, which is now only limited by the intermediate-frequency (IF) bandwidth of the network analyzer, e.g., 3 kHz for the HP 8510, resulting in a dynamic range for the higher harmonics of more than 100 dB.

B. Independent Control of BB, Fundamental, and Second-Harmonic Impedance

In order to facilitate independent control of the BB, fundamental, and second-harmonic impedances at the device terminals, a new multiplexer board has been developed (Fig. 3). This board decouples the frequency components of interest through the use of a multistub network, which employs $\lambda/4$ lines at f_0 and $2f_0$ to obtain high isolation between the fundamental and second-harmonic signal path (>30 dB). It is important to mention that this network presents also low-reflection coefficients at the DUT for the frequency spectrum outside the controlled frequency bands at BB, f_0 , and $2f_0$. This is essential to avoid oscillations when measuring devices with a high f_{\max} . The feed line in Fig. 3 provides the required dc biasing and BB

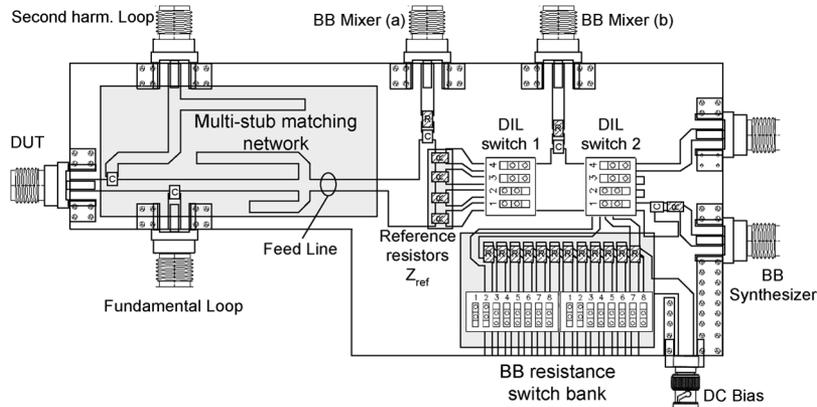


Fig. 3. Multiplexer board used to split the DUT signal in BB fundamental and double frequency component using a multistub network. The BB impedance (dc-coupled) can be controlled via the resistive switch bank. The resulting impedance can be measured by the HP 8510 VNA.

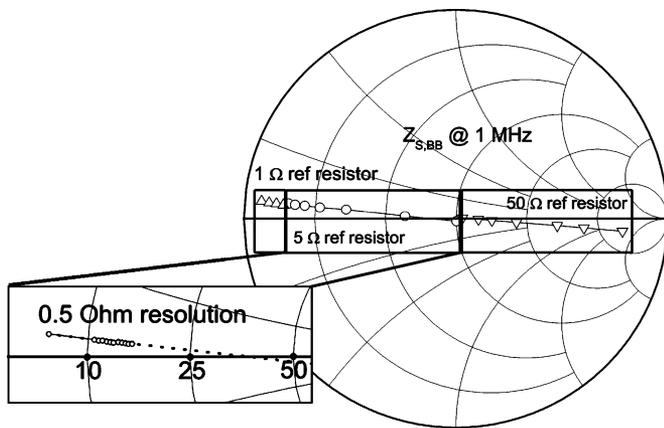


Fig. 4. Various BB impedances at the DUT reference plane, measured at 1 MHz using the BB impedance calibration procedure. The reference resistance used for the different ranges is also indicated, and the zoomed window shows the 0.5- Ω resolution.

impedance control, avoiding the need for a decoupling coil. This allows the use of large tone spacing (Δ_f) without suffering from BB inductance, which would yield IM3 asymmetry [15] (this problem often appears when using conventional bias-Tees in linearity measurements). The resistor switch bank provides excellent control of the BB impedance by using quality switches with low-inductance resistors. This facilitates a 0.5- Ω resolution in the control of the BB impedance (see Fig. 4). This high resolution is required in the linearity optimization procedure of bipolar transistors as described in [9]. Note that the total phase shift of the BB reflection coefficient (including connecting cables) is limited to 5.3 $^\circ$ /MHz. The multiplexer board also facilitates the use of an external electronically controlled load or a modulated BB signal [16] (see Fig. 3). The BB signals are sensed over the reference resistor (Fig. 3). The value of this resistor can be set to 1, 5, and 50 Ω to maximize the measurement accuracy of the BB impedance.

When the lowest BB impedance is required, this reference resistor can also be short-circuited by a switch. The BB (envelope) signals sensed over the reference resistor (available at the outputs *BB mixer a* and *BB mixer b* in Fig. 3) are then up-converted by low-frequency mixers to the IF of the HP 8510 receiver (20 MHz). In this way, the BB signals can also be mea-

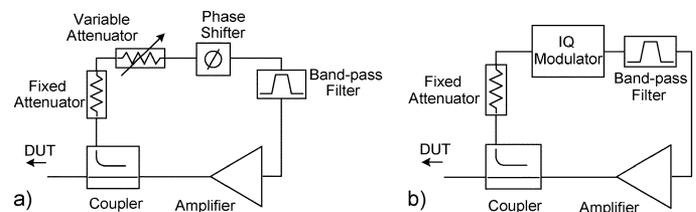


Fig. 5. (a) Conventional active loop using separate amplitude and phase adjustment. (b) Block diagram of implemented active loop combining the phase and amplitude adjustment in on circuit block.

sured by the HP 8510 unit. This facilitates the calibrated measurement of the complex source and load BB reflection coefficients offered to the DUT without the need of additional equipment. The corrected BB loading conditions are calculated, from the raw sensed data, using the calibration formulas in [13].

C. Active Loads With Low Electrical Delay

The active loads are implemented using the closed-loop architecture of Fig. 5. By adjusting the phase and magnitude in the signal path, the complete Smith chart can be covered. The biggest advantage of the loop architecture is that it provides an almost constant reflection coefficient, versus power and frequency, for not too excessive wideband signals. This is important since the fundamental and the nearby distortion components (i.e., third- and fifth-order intermodulation products) must experience the same reflection coefficient to mimic a realistic circuit condition. The only limitation of the loop topology is set by the electrical length of the loop yielding a $\angle\Gamma$ variation versus frequency. Consequently, the physical dimensions of the loop should be minimized. For this purpose the conventional loop architecture [Fig. 5(a)], using a separate phase shifter and attenuator, is replaced by the more compact implementation of Fig. 5(b) which utilizes a custom developed in-phase quadrature modulator to implement the phase and magnitude control. As a result, the electrical length of the loop is minimized. The modulator is realized using highly linear pin diodes,⁴ providing fast settling times for high-speed measurements.

⁴BAP70-03 Data Sheet. [Online]. Available: <http://www.semiconductors.philips.com>

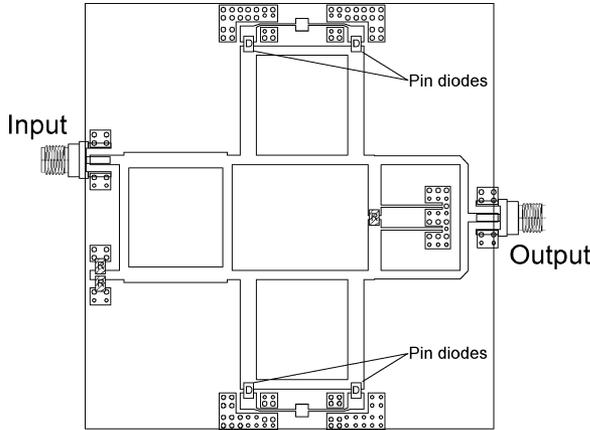


Fig. 6. In-phase quadrature modulator used for controlling the phase and amplitude of the wave in the loop at f_0 .

The final design of the modulator is shown in Fig. 6. A fixed attenuator is used to optimize the power levels in the loop. The loop filter is added to eliminate gain outside the intended frequency band, which might trigger unwanted oscillations.

IV. SYSTEM PERFORMANCE

A. Power Handling and System Linearity

To characterize the power handling and linearity of the active loads, we perform a two-tone power sweep (tone spacing 200 kHz) over a calibration “Thru,” while the output active loop at f_0 is set to provide a high reflection coefficient ($|\Gamma_L| = 0.91$) for four different angles at the DUT reference plane of the setup in Fig. 2. The magnitude of the resulting Γ_L versus the power of wave b_2 (P_b) at the DUT reference plane is given in Fig. 7(a). Note that the loops present an almost constant and therefore linear reflection coefficient up to 25 dBm for the various conditions. The related effective third-order intercept (IP_3) of the active loops at the DUT reference plane is measured and computed as follows:

$$IP_{3a2} = P_{a2,\text{fund}} + \frac{P_{a2,\text{fund}} - P_{a2,\text{IM3}}}{2} \quad [\text{dBm}] \quad (1)$$

where P_{a2} represents the power of the a_2 wave (output wave incident to DUT). Fig. 7(b) shows the measured IP_{3a2} for the four different angles of the reflection coefficient.

This data can be considered a close to worst-case condition ($|\Gamma_L| \approx 1$), since for lower magnitudes of the reflection coefficient, the required power from the loop amplifier drops significantly, relaxing the linearity constraints. For the situation that we aim to characterize, linear devices with different (lower) $|\Gamma_L|$ conditions, we can derive some qualitative linearity specifications of the system. For this purpose, we consider the incident a_2 and reflected b_2 waves at the output of the device. Through these, we can relate the power of the IM3 component of the a_2 wave ($P_{a2,\text{IM3}}$) to the power delivered to the load (P_{load}) for any given load reflection coefficient at the DUT reference plane.

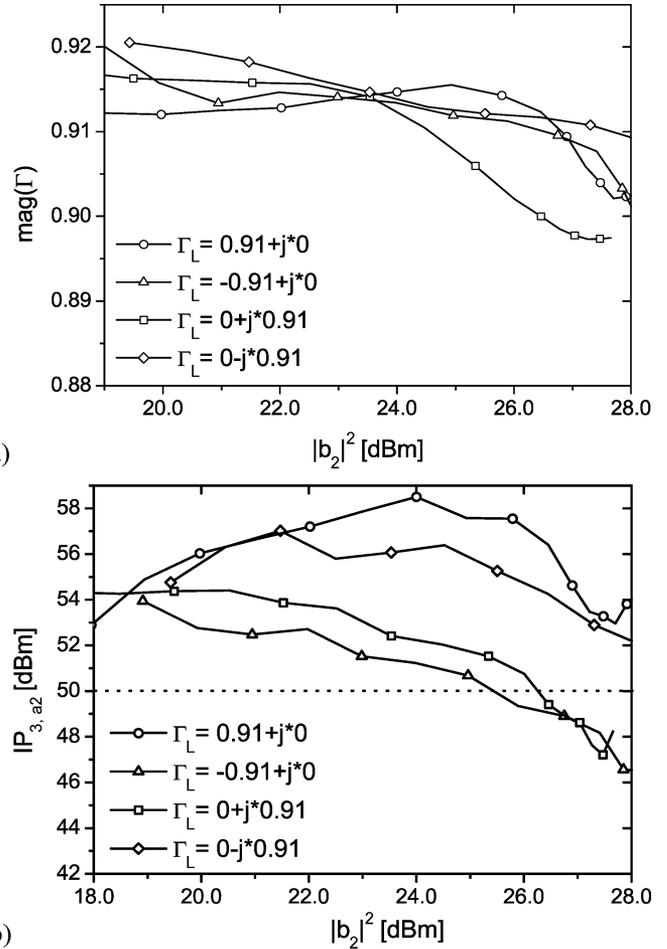


Fig. 7. (a) Magnitude of load reflection coefficient versus power of the b_2 wave at the DUT reference plane, for different Γ_L values. (b) Third-order intercept of output active loop versus power of the b_2 wave measured at the DUT reference plane for different Γ_L values.

If we assume that all power levels are given in dBm, we can write the following expression:

$$P_{a2,\text{IM3}} = 3P_{a2,\text{fund}} - 2IP_{3,a2} = 3 \left[P_{\text{load}} + 10 \log \left(\frac{|\Gamma_L|^2}{1 - |\Gamma_L|^2} \right) \right] - 2IP_{3,a2} \quad [\text{dBm}] \quad (2)$$

where $IP_{3,a2}$ represent the third-order intercept of the active loop at the DUT reference plane for the a_2 wave. From Fig. 7, we can conclude that, for power levels below 25 dBm, the $IP_{3,a2}$ of the active loops is always better than 50 dBm. Using this value as a constant in (2), we can plot the IM3 component generated by the active loop, which will set a lower limit on the measurable components for a given $|\Gamma_L|$, as shown in Fig. 8. In this plot, we assume that the nonlinearity of the loop is the only limitation in the detection of the IM3 components where we have assumed the worst case scenario, namely, that $b_2 \approx a_2$. Note that, when the magnitude of the reflection coefficient ($|\Gamma_L|$) is lower, the IM3 contribution due to the active loop decreases drastically

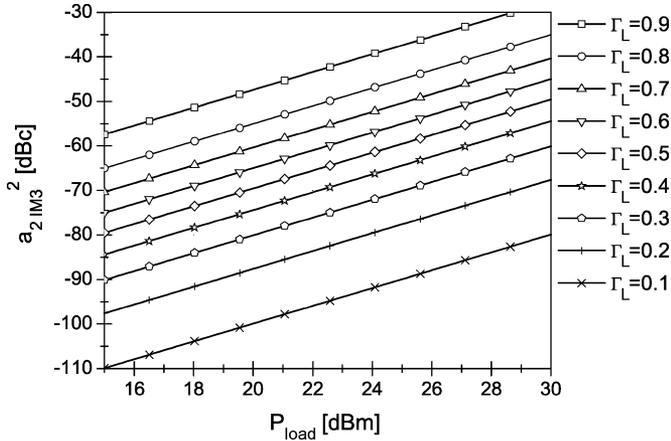


Fig. 8. Calculated power of the IM3 component of the a_2 wave in dBc versus power delivered to the load for various $|\Gamma_L|$ conditions.

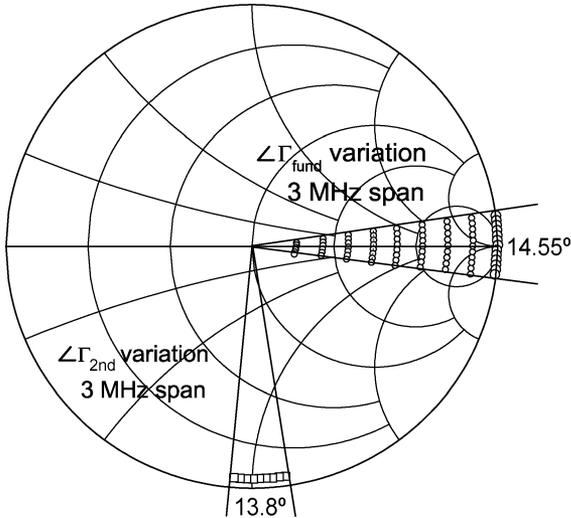


Fig. 9. Measured $\Delta\Gamma$ variation with frequency at the DUT reference plane for the active loop at the output (frequency span 3 MHz).

since less loop power is required, allowing the proper detection of much smaller components.

B. Bandwidth Consideration for Modulated Signals

For wideband-modulated signals, the system components in the DUT signal path must be kept as compact as possible to minimize the electrical delay and, consequently, the $\Delta\Gamma$ variation with frequency. This requirement comes from the need to provide realistic reflection coefficients when employing wideband-modulated signals. The achieved $\Delta\Gamma$ variation with frequency of the active loads at the DUT reference planes (Fig. 2) is shown in Fig. 9. To place these results better in perspective, it is useful to mention that the $\Delta\Gamma$ variation with frequency of commercial active load–pull systems is in the order of $30^\circ/\text{MHz}$. (passive load–pull setups can provide in principle a lower $\Delta\Gamma$ variation with frequency, but fail to provide the high magnitude for the harmonic reflection coefficients). The individual contributions to the $\Delta\Gamma$ variation with frequency of the various system components are summarized in Table I. The table shows that

TABLE I
ACTIVE LOOP $\Delta\Gamma$ VARIATION

	$\Delta\Gamma$ variation [$^\circ/\text{MHz}$]
	Input / Output
Probe + cable	0.9 / 0.9
Coupler section	1.2 / 1.0
Diplexer	0.4 / 0.4
Active loop f_0	2.55 / 2.55
Active loop $2f_0$	2.3 / 2.3
Total f_0	5.05 / 4.85
Total $2f_0$	4.8 / 4.6

the loop at $2f_0$ achieves a smaller $\Delta\Gamma$ variation with frequency than the fundamental loop. This is mostly due to the reduced dimensions of the in-phase quadrature modulator (see Fig. 6). To highlight the degrading effects of the $\Delta\Gamma$ variation with frequency on the device linearity when using wideband-modulated signals, we consider the out-of-band linearization technique for a bipolar device [3], [9].

This technique (see also Section II), when applied to a bipolar device, can result in frequency-independent IM3 cancellation, provided that the optimum out-of-band terminations are applied at the BB and double frequencies. For this reason, the only practical parameter limiting the wideband linearity performance of an out-of-band optimized bipolar device will be the $\Delta\Gamma$ variation with frequency. When considering two-tone test conditions (Fig. 1), it is clear that, for a tone spacing Δf between the fundamental tones, the spectrum of interest at the double frequency is twice as large ($2\Delta f$). This indicates that, at first approximation, the $\Delta\Gamma$ variation at the second harmonic is the parameter that mostly affects the bandwidth of the cancellation technique.

To evaluate the impact of the $\Delta\Gamma$ variation with frequency on the achievable bipolar device linearity, we consider the simulation setup of Fig. 10. In this setup, an idealized RF bipolar transistor is represented by the Gummel Poon model in Agilent's ADS. The device is matched for its optimum gain at the fundamental frequency (f_0), while the linearity is optimized through the BB and second-harmonic terminations. To mimic the $\Delta\Gamma$ variation with frequency, we have used an ideal $50\text{-}\Omega$ transmission line at the input of the device;⁵ note that this line will only rotate the reflection coefficients as a function of its electrical length but does not change the magnitude of the intended reflection coefficients. Next, the electrical length of this transmission line is stepped up in value to provide the different values of the $\Delta\Gamma$ variation with frequency. When considering the results of the HB simulations, we see from Fig. 11 that the power gain (G_p) only weakly depends on the $\Delta\Gamma$ variation with frequency. In contrast, when we consider the influence of the $\Delta\Gamma$ variation on the device linearity, we see a large impact [see Fig. 12(a)]. Here, the constant third-order output intercept point (OIP₃) trace versus Δf represents the ideal condition ($0^\circ/\text{MHz}$). Increasing the $\Delta\Gamma$ variation with frequency by stepping up the electrical length of the transmission line at the input of the DUT considerably reduces the bandwidth of the IM3 cancellation, yielding linearity degradation. For comparison, the performance achievable with a system with $30^\circ/\text{MHz}$ is also given.

⁵Here, we have only used the TL at the input of the device to simplify the analysis.

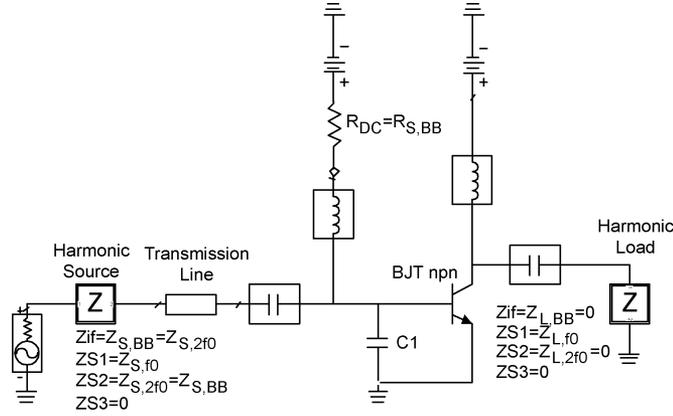


Fig. 10. Agilent's ADS simulation setup for bipolar device linearity simulation.

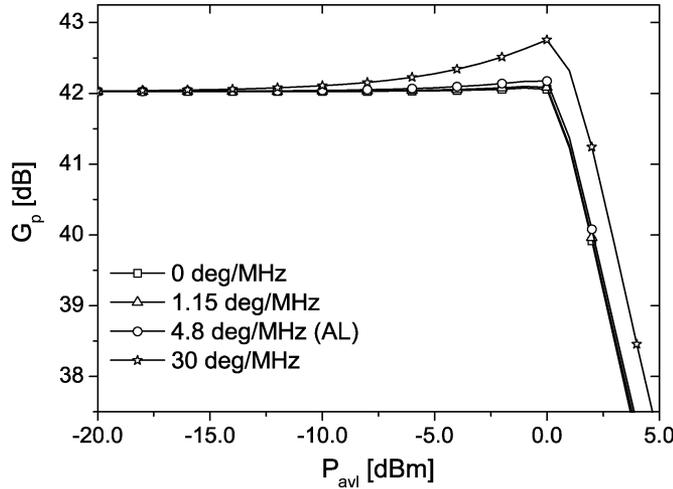


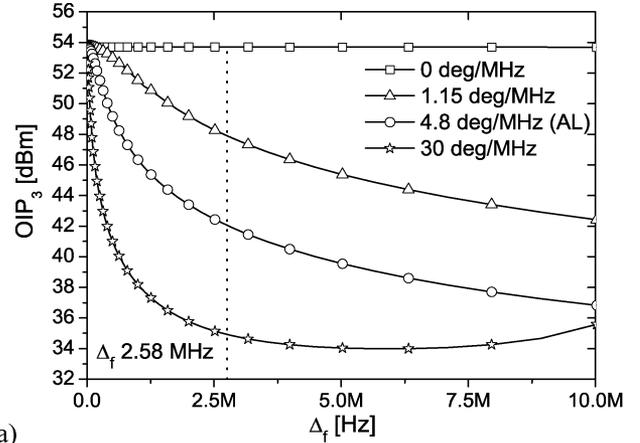
Fig. 11. Simulated power gain (G_p) versus power available from the source (P_{avl}) considering different conditions of $\Delta\Gamma$ variation with frequency (0, 1.15, 4.8, 6, and 30 °/MHz).

The impedances seen at the second harmonic by the device (source side) are shown for the Delft system (AL) and the commercially available system in Fig. 12(b).

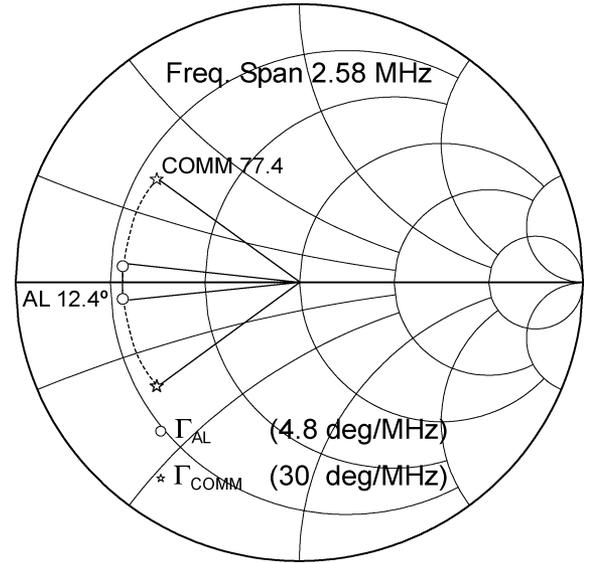
For the commercial system, we observe that high linearity can only be achieved in a very narrow bandwidth. At large bandwidths, the third-order output intercept point starts to increase again for a tone spacing Δ_f in the order of 10 MHz since for this tone spacing, with the given $\Delta\Gamma$ variation versus frequency (30 °/MHz), the reflection coefficient of the second harmonic has turned around the entire Smith chart, returning to its original values. It is obvious that this effect has no practical value when dealing with modulated signals, since these can be considered to be composed out of a very large number of tones with various frequency spacing. The marker at 2.58 MHz is used to provide an indication of the maximum linearity achievable for this fictive bipolar device under an IS-95 CDMA signal (bandwidth of 1.29 MHz).

V. EXPERIMENTAL OUT-OF-BAND LINEARIZATION RESULTS

The hardware presented in the previous sections allows the Delft system to perform some unique measurements in the characterization and optimization of device linearity for power amplifier applications. To illustrate the features of the realized



a)



b)

Fig. 12. (a) Simulated OIP3 point for the device of Fig. 11 versus tone spacing (Δ_f) for different conditions of the $\Delta\Gamma$ variation with frequency at $P_{avl} = -28$ dBm. The case for the realized active loop (AL) has been indicated. (b) $\Delta\Gamma$ variation with frequency for 2.58-MHz bandwidth for active loop (AL) and reference commercial system.

system, we consider both bipolar junction transistor (BJT) as well as field-effect transistor (FET) devices in (inverse) class-AB operation. The motivation to address both device types is given by the fundamentally different electrical behavior of these devices, resulting in different out-of-band impedance requirements for optimum linearity.

A. Two-Tone BJT Linearity Optimization

Bipolar devices are characterized by their exponential behavior. This well-defined behavior allows analytical considerations for the optimum out-of-band source and load conditions when the device is operated far from compression. Consequently, it was shown [17] that, for a bipolar device in class-AB operation, frequency-independent IM3 cancellation can be achieved when the following conditions are satisfied:

$$\begin{aligned} Z_{S, BB} &= Z_{S, 2nd} = \frac{\beta_F}{2g_m} \\ I_{cq, opt} &= V_T \frac{C_{jE}}{2\tau_F} \end{aligned} \quad (3)$$

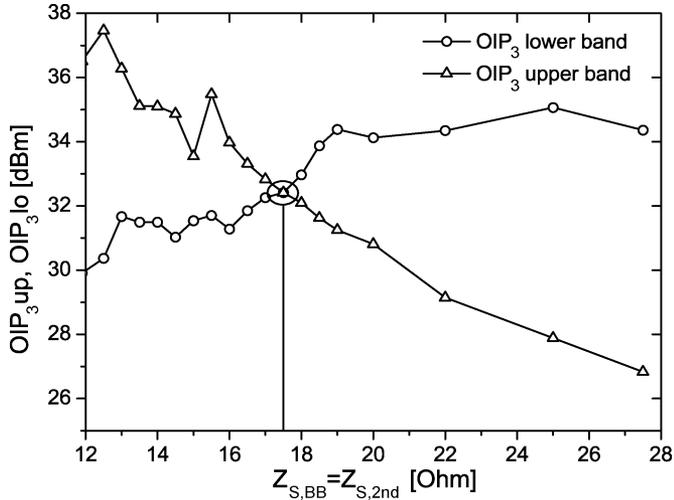


Fig. 13. Measured maximum third-order output intercept point (OIP_3) levels for upper and lower IM3 components versus resistive $Z_{S,BB} = Z_{S,2nd}$ using a swept I_{cq} bias conditions ($f_0 = 2.14$ GHz, $\Delta f = 0.5$ MHz).

when

$$Z_{L,BB} = Z_{L,2nd} = 0$$

where

$Z_{S,BB}$	source BB impedance;
$Z_{S,2nd}$	source second-harmonic impedance
$Z_{L,BB}$	load BB impedance;
$Z_{L,2nd}$	load second-harmonic impedance;
$I_{cq,opt}$	optimum quiescent collector current;
g_m	transconductance;
β_F	forward current gain of the transistor;
C_{jE}	emitter–base capacitance in the operating point;
τ_F	forward delay time in the operating point.

As a result of these relations, when aiming for frequency-independent IM3 cancellation in a given technology, the out-of-band impedances and quiescent current are fixed. Setting the out-of-band terminations to these values leads to significant improvements in linearity for both the lower and upper IM3 sidebands. The use of (3), however, assumes an accurately precharacterized device and associated model, while one of the goals of load-pull measurements is to circumvent these needs.

In view of this, in [15], it was shown that the out-of-band impedances can cause asymmetry between the upper and lower intermodulation distortion products. We have utilized this phenomenon to define an experimental procedure to determine the optimum out-of-band loading conditions [9]. In this procedure, for a low-power two-tone input signal, we sweep the quiescent current of a ($22 \times 2.2 \mu\text{m}^2$ GaAs Skyworks HBT) and measure the maximum in third-order output intercept point for both lower and upper IM3 bands while increasing the ohmic value of $Z_{S,BB} = Z_{S,2nd}$ (Fig. 13).

The point where the third-order output intercept point for both the lower and upper bands are equal results in the best linearity and provides us the specific impedance and quiescent current for

the given device that results in frequency-independent IM3 cancellation. Fig. 14 clearly shows that satisfying the conditions of (3) indeed results in the best linearity performance at low power levels. This becomes evident when comparing with the classic class-AB condition (Fig. 14: trace ref, all out-of-band termination conditions short-circuited) with the $Z_{S,BB} = Z_{S,2nd} = 17.5 \Omega$ condition (Fig. 14: trace t1). To improve the linearity of the bipolar device close to compression and hence to improve its power-added efficiency (PAE), it was shown [9] that keeping $Z_{S,BB} = Z_{S,2nd}$ at its optimum value, while increasing the quiescent current, yields a IM3 sweet spot close to the compression point. Note that the presence of the sweet spot moves now the rising slope of the IM3 trace to a higher power level, which results in an improved adjacent channel power (ACPR) versus output power when using complex modulated signals.

To further improve both efficiency and linearity levels close to the compression point of the device, we increase $Z_{S,BB}$ and lower the quiescent current. This violates the wideband cancellation condition, which we can correct for, in a restricted bandwidth, by allowing now a complex second-harmonic source termination.

The required complex $\Gamma_{S,2nd}$ is found by a source-pull on the bipolar device (traces t4 and t5). As a result, the sweet spot is moved even closer to compression (Fig. 14), extending the linear operation to even higher power levels. The lower quiescent current and the better linearity at higher power levels translate directly into a significant efficiency improvement of the amplifier, as will be shown in Section V-B.

B. BJT Linearity Optimization Using Wideband Signals

As mentioned before, modern communication modulation schemes present a higher peak to average ratio than two-tone signals. For this reason, the achieved linearity improvement for two-tone stimulus has to be also tested using a realistic digital modulated signal.

Since the Delft system was developed in order to facilitate the use of wideband signals, an IS-95 CDMA signal is used to measure the achieved linearity and efficiency level for loading conditions of traces t3, t4, and t5. In Table II, we summarize the achieved P_{out} and efficiency for these cases when using an adjacent channel power constrain of (-45 dBc). The achieved results of Table II show the same trend found in the two-tone analysis, shown in Fig. 14.

C. FET Linearity Optimization

The FET linearity characterization and optimization have been performed using Philips LDMOS devices of different technology generations. The gate length of the tested devices of these generations (Gen 2 to Gen 6) is 1.8 mm. In contrast with bipolar devices, there is no analytical expression for the optimum biasing current and out-of-band impedances available for LDMOS devices.

For this reason, we will have to use an experimental procedure for their linearity/efficiency optimization. The biasing point for the various generations is set close to the threshold and is summarized in Table III.

In [18], it was first shown that out-of-band IM3 cancellation technique at the input of a device could provide linearity im-

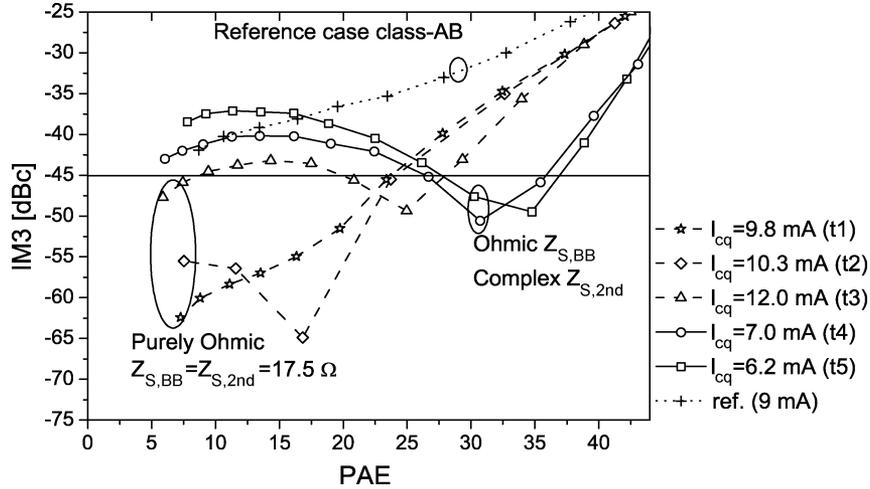


Fig. 14. Third-order intermodulation versus PAE for the various biasing cases and the reference class-AB case.

TABLE II
CDMA P_{out} AND EFFICIENCY AT IM3 OF -45 dBc

I_{cq}	12 mA (t3)	7 mA (t4)	6.2 mA (t5)
$P_{\text{out CDMA}}$	9.2 dBm	10.2 dBm	10.6 dBm
PAE_{CDMA}	21%	29%	31.5%

TABLE III
LDMOS BIASING POINT

	V_d [V]	I_d [mA/mm]
Gen2	26	3.5
Gen4	26	5
Gen5	28	7.5
Gen6	28	7.5

improvements close to the compression point of LDMOS devices. Moreover, in [19], it was proven that BB shorts in the input and output combined with an open condition for both $Z_{L,2\text{nd}}$ and $Z_{S,2\text{nd}}$ yields the best LDMOS efficiency for a specified linearity level. In this study, we compare the linearity performances versus output peak envelope power (PEP) of the various Philips LDMOS generations (Fig. 15).

The initial optimum load and source conditions for the fundamental frequency (f_0) were provided by Philips Semiconductors, Nijmegen, The Netherlands. The source and load BB impedances are set to a short condition. The figure clearly shows the linearity improvement of each successive LDMOS generation. It should be mentioned that, here also, the rising slope in IM3 versus output power close to compression is a good indicator of the linearity. Shifting this slope to higher power levels will improve the adjacent channel power for complex modulated signals at these levels. With the above in mind, we have used our Deflt system to optimize the second-harmonic out-of-band terminations of the Gen 6 device, resulting in the use of an open-open condition for $Z_{L,2\text{nd}}$ and $Z_{S,2\text{nd}}$ (trace Gen6_{OO}). If we use a -45 -dBc reference level to qualify the achieved shift in power level for the upgoing IM3 slope, we observe 2-dB improvement in PEP.

In Fig. 16, the linearity levels for the various generations are plotted versus PAE. This plot clearly quantifies the efficiency

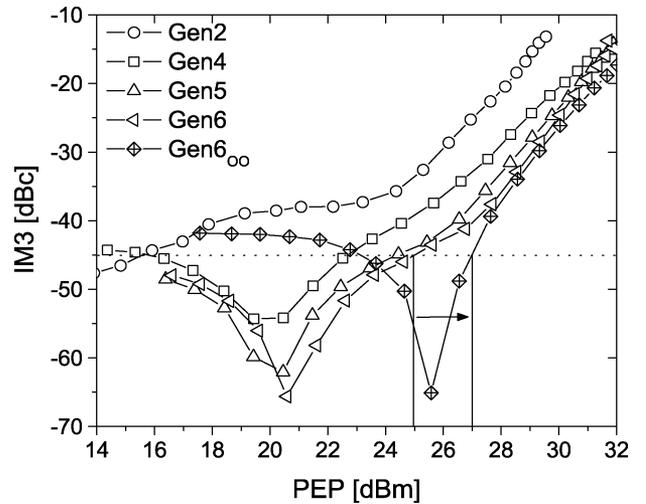


Fig. 15. Measured IM3 levels of various LDMOS generations, versus PEP.

improvement for a given linearity level of the various device generation.

When using the optimized second-harmonic conditions for a Gen 6 device (Fig. 16: trace Gen6_{OO}) an additional improvement as high as 10% in efficiency can be reported for a linearity level of -45 dBc.

D. FET Linearity Optimization Using Wideband Signals

As shown for the bipolar device, for LDMOS devices also, the linearity improvement found under two-tone excitation is verified using a digital modulated signal (IS-95). In Fig. 17, the adjacent channel power (ACP) of the various generations is shown versus power added efficiency. Also, here we find the same trend as with the IM3 measurements, while the open-open second-harmonic conditions (Gen6_{OO}) result in the rather spectacular efficiency value of 44% at an adjacent channel power reference level of -45 dBc. To the best of the authors' knowledge, this is a record value for "class-AB" operated LDMOS devices without digital predistortion.

In Fig. 18, we show the output spectrum of the IS-95 CDMA signal for the various generations of LDMOS generations and

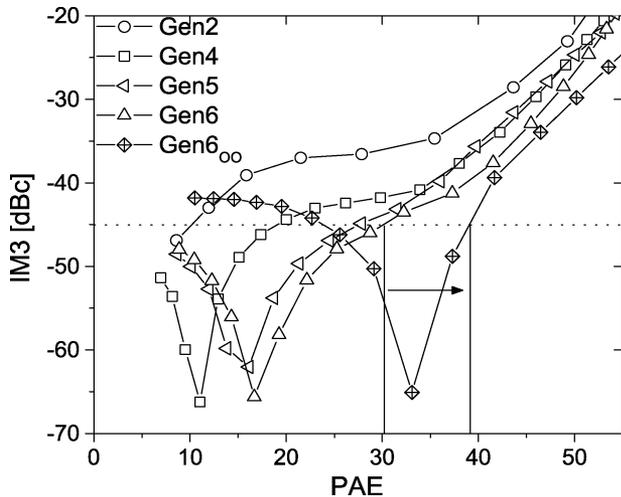


Fig. 16. Measured IM3 levels of various LDMOS generations versus two-tone efficiency (PAE).

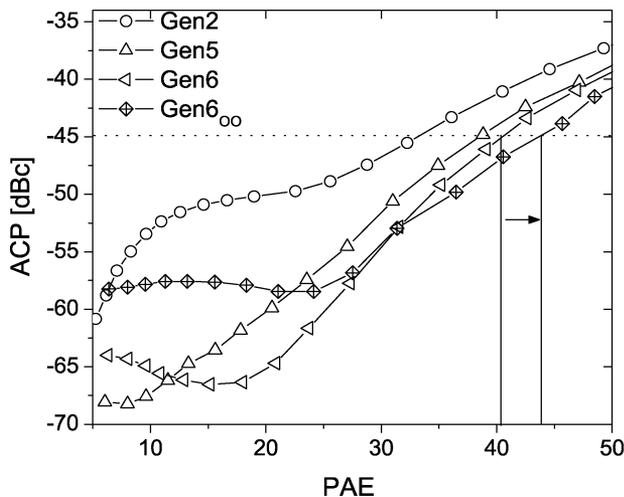


Fig. 17. Measured ACP levels of various LDMOS generations versus CDMA efficiency (PAE).

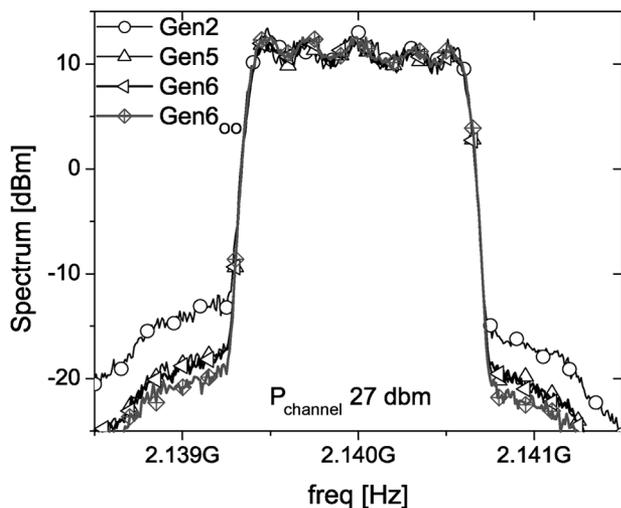


Fig. 18. Output spectrum of CDMA IS-95 signal for the various LDMOS generations.

for the optimized Gen6_{oo} for a channel output power level of 27 dBm.

VI. CONCLUSION

In this study, we have presented a custom load–pull setup entirely optimized for on-wafer device linearity characterization. To support this goal, the impedances at the fundamental, BB, and second-harmonic frequencies at both the source and load sides are independently controlled and accurately measured using real-time calibration techniques.

The phase variation of the reflection coefficients offered to the DUT is minimized by reducing all the electrical delays in the system. This results in very realistic (circuit-like) loading conditions for the active device when performing linearity testing with wideband-modulated signals (e.g., CDMA).

The resulting system performance in terms of the maximum measurable linearity has been carefully verified both by measurements and analysis as function of power, matching conditions, and bandwidth and found to be compatible with the current requirements in highly linear applications (e.g., handsets and base stations). The unique capabilities of the system for linearity optimization are demonstrated using the out-of-band linearization technique for a (nonproduction) Skyworks GaAs HBT device. By following a carefully chosen sequence of steps to define: the optimum bias, fundamental, BB, and second-harmonic loading conditions an efficiency of 31.5% was achieved for the IS-95 signal using an adjacent channel power level constraint of -45 dBc. Even more exciting results are found when monitoring the steady performance increase over the various Philips LDMOS generations for base station applications yielding a state-of-the-art linearity efficiency performance of 40%.

By applying second-harmonic input and output tuning on the latest GEN6 LDMOS generation, an efficiency of 44% was achieved for an IS-95 signal with an adjacent channel power reference level of -45 dBc. To the best of the authors' knowledge, this is a record value for a “class-AB” operated LDMOS device.

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