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Design of Microwave GaAs MESFET's for Broad-Band Low-Noise Amplifiers

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***Abstract*—As a basis for designing GaAs MESFET's for broad-band low-noise amplifiers, the fundamental relationships between basic device parameters, and two-port noise parameters are investigated in a semiempirical manner. A set of four noise parameters are shown as simple functions of equivalent circuit elements of a GaAs MESFET. Each element is then expressed in a simple analytical form with the geometrical and material parameters of this device. Thus practical expressions for the four noise parameters are developed in terms of the geometrical and material parameters.**

Among the four noise parameters, the minimum noise figure F_{min}, and equivalent noise resistance R_n, are considered crucial for broad-band low-noise amplifiers. A low R_n corresponds to less sensitivity to input mismatch, and can be obtained with a short heavily doped thin active channel. Such a high channel doping-to-thickness (N/a) ratio has a potential of producing high power gain, but is contradictory to obtaining a low F_{min}. Therefore, a compromise in choosing N and a is necessary for best overall amplifier performance. Four numerical examples are given to show optimization processes.

I. INTRODUCTION

THE GaAs Schottky-barrier gate field effect transistors (GaAs MESFET's) have demonstrated excellent noise and gain performance at microwave frequencies through K band [1]. The excellent microwave performance of GaAs MESFET's is certainly related to their channel properties. GaAs MESFET's to be used for broad-band low-noise amplifier applications, must have special requirements on their channel properties for optimum performance. The purpose of this paper is to investigate the fundamental relationships between the noise and small-signal properties, and the basic channel parameters of GaAs MESFET's. This information should be useful as a basis for device design.

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II. REPRESENTATION OF NOISE PROPERTIES

A. Noise Parameters

From the circuit point of view, the GaAs MESFET can be treated as a black box of noisy two port. The noise properties of such a black box are then characterized by a set of four noise parameters in the binomial form [2]. A derivation of this form can be written as

$$F = F_{\min} + \frac{R_n}{R_{ss}}\left[\frac{(R_{ss}-R_{op})^2+(X_{ss}-X_{op})^2}{R_{op}^2+X_{op}^2}\right] \quad (1)$$

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where

F	noise figure,
$F_{\min}$	minimum (or optimum) noise figure,
R_n	equivalent noise resistance,
R_{ss}	signal source resistance,
R_{op}	optimum signal source resistance,
X_{ss}	signal source reactance,
X_{op}	optimum signal source reactance.

In this expression, $F_{\min}$, R_n, R_{op}, and X_{op} are the characteristic noise parameters of the device. Since the noise figure F is a function of its driving source impedance, the minimum noise figure $F_{\min}$ is achieved only when the driving source impedance is exactly at the optimum signal source impedance.

As has been well known, (1) can be represented on the source impedance Smith chart as a family of circles, each of which corresponds to a constant F value [3]. The spatial distance between two circles is related to R_n. The greater R_n corresponds to the shorter distance. In other words, the noise figure of a device with a small value of R_n is relatively insensitive to the variation in the signal source impedance. Thus small R_n is essential for a device to be used in a broad-band amplifier where a large tolerance is desirable in the input match. Furthermore, as will be seen later, R_n has a close relationship with power gain. Usually, the smaller R_n value corresponds to the higher gain in a given gate structure. In the design of a low-noise MESFET, therefore, obtaining a low R_n should be considered to be just as crucial as achieving a low $F_{\min}$.

It may be noted that an equivalent expression of (1), in terms of the source-reflection coefficient, is found elsewhere [4]. This expression is based on the circuit analysis using the s parameters. The s-parameter representation would be convenient to use in conjunction with the test facilities available for two-port investigation these days. However, the impedance parameter would provide us with direct insight into the operation of a device under consideration. Therefore, the noise parameters in the impedance form are adopted in this paper. If necessary, the noise parameters of this form can be transformed into other forms in a straightforward manner.

B. Noise Equivalent Circuit

It has been well accepted that the noise properties of a GaAs MESFET would be described by an equivalent circuit as shown in Fig. 1 [5], if the effect of reactive parasitic elements on the noise performance could be ignored. The major reactive parasitic elements are lead inductances and header stray capacitances. As the operating frequency increases, the impedance of such external elements may become comparable to those of the corresponding internal elements, and then the reactive parasitic effects are no longer negligible. Such a critical frequency, that the reactive parasitic effect begins to participate in the determination of the noise performance parameters, may vary from one noise parameter to another for a given device. For example, the critical frequency for $F_{\min}$ may be much higher than those for R_n, R_{op}, and X_{op}, analogous to microwave bipolar transistors [6].

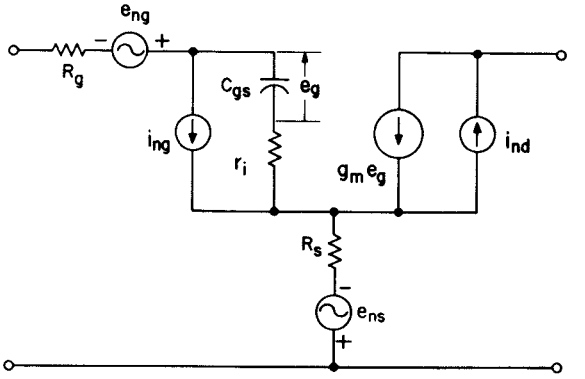

Fig. 1. Noise equivalent circuit of GaAs MESFET's. g_m is the transconductance which is assumed to be constant over the frequency range of interest. Element C_{gs} is the gate-source capacitance, r_i, the associated charging resistance, R_g, the ac gate metallization resistance, and R_s, the total source resistance series. Noise sources i_{ng}, i_{nd}, e_{ng}, and e_{ns} represent the induced gate noise, drain-circuit noise, thermal noise of R_g, and R_s, respectively.

III. Formulation of Noise Parameters in Terms of Device Geometrical and Material Parameters

A. Experimental Procedure and Results

Relationships between the noise parameters and equivalent circuit elements have been given in rigorous but complicated forms [5]. For practical purposes, however, it would be much more convenient if simple analytical forms of such relationships were available with reasonable accuracy.

In order to carry out this search, GaAs MESFET's with nominal gate length of 2 μm were used in the experiments described below. The MESFET's were mounted in the package which had a total input lead inductance of approximately 1 nH, a total output lead inductance of approximately 1 nH, a common-source lead inductance of approximately 0.12 nH, and a header stray capacitance of approximately 0.08 pF at both input and output [7]. As a result of such parasitic element values, these devices nearly satisfied the aforementioned requirement for possible elimination of the reactive parasitic effects on any of the four noise parameters at a test frequency of 1.8 GHz. Therefore, only the equivalent circuit elements shown in Fig. 1 will be referred to in the analyses described later on.

Table I shows the geometrical and material parameters of the six GaAs MESFET's used in the experiments. In Table I, N is the free carrier concentration in the active channel in units of 10^{16} cm^{-3}, L is the gate length in micrometers, a is the active channel thickness in micrometers, Z is the total device width in millimeters, and z is the unit gate width in millimeters. Since z was 0.25 mm for all devices, each device had either two or six paralleled unit

TABLE I
GEOMETRICAL AND MATERIAL PARAMETERS OF SAMPLE GaAs MESFET's

	DEVICE	N ($10^{16}cm^{-3}$)	L (μm)	a (μm)	Z (mm)	z (mm)
a :	K864-1-02	11.0	1.85	0.174	0.5	0.25
b :	K976-1-04	7.5	1.85	0.40	0.5	0.25
c :	K949-1-12	5.5	1.85	0.44	0.5	0.25
d :	K949-3-02	5.5	2.3	0.35	1.5	0.25
e :	C75B-1-05	5.0	2.3	0.46	0.5	0.25
f :	C75B-3-04	5.0	2.3	0.38	1.5	0.25

TABLE II
MEASURED VALUES OF NOISE PARAMETERS AND EQUIVALENT CIRCUIT ELEMENTS OF SAMPLE GaAs MESFET's

DEVICE	F_{min} (dB)	R_n (Ω)	R_{op} (Ω)	X_{op} (Ω)	g_m (U)	C_{gs} (pF)	R_g (Ω)	R_s (Ω)
a	1.80	31	40	85	0.031	1.0	2	8.5
b	1.29	-	45	145	0.021	0.65	2	6
c	1.56	-	45	140	0.019	0.62	3	6
d	1.70	13.3	23	47	0.047	2.0	1	3.5
e	1.73	94	50	125	0.018	0.68	2	8
f	2.04	15.3	35	45	0.044	2.2	4	3.5

gates. These devices were an early version of the low-noise GaAs MESFET reported elsewhere [8]. An epitaxial film, as the active channel, was grown directly on a semi-insulating substrate in the first four devices. In the last two devices, however, there was an additional undoped buffer layer between the substrate and active layer.

Four noise parameters F_{min}, R_n, R_{op}, and X_{op} were measured at 1.8 GHz under optimum gate-bias condition for each device, using the standard technique [9]. Equivalent circuit elements g_m, C_{gs}, R_g, and R_s were evaluated from the s-parameter measurement taken as a function of frequency under the zero gate-bias condition, in a similar way to that described in [10]. All the above parameters were measured at room temperature. The results are shown in Table II.

B. Derivation of Expressions for Noise Parameters in Terms of Equivalent Circuit Elements

It was assumed that the four noise parameters could be expressed in terms of equivalent circuit elements as follows:

$$F_{min} = 1 + k_1 f C_{gs} \sqrt{\frac{R_g + R_s}{g_m}} \tag{2}$$

$$R_n = \frac{k_2}{g_m^2} \tag{3}$$

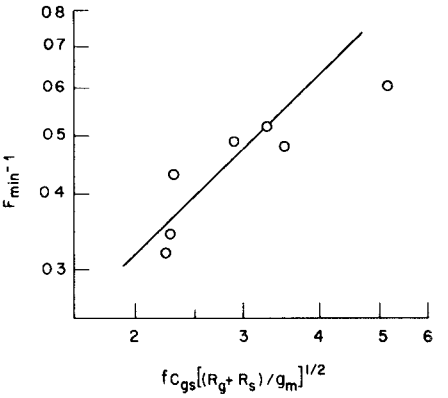

Fig. 2. Correlation between the minimum noise figure F_{min} and equivalent circuit elements, C_{gs}, g_m, R_g, and R_s.

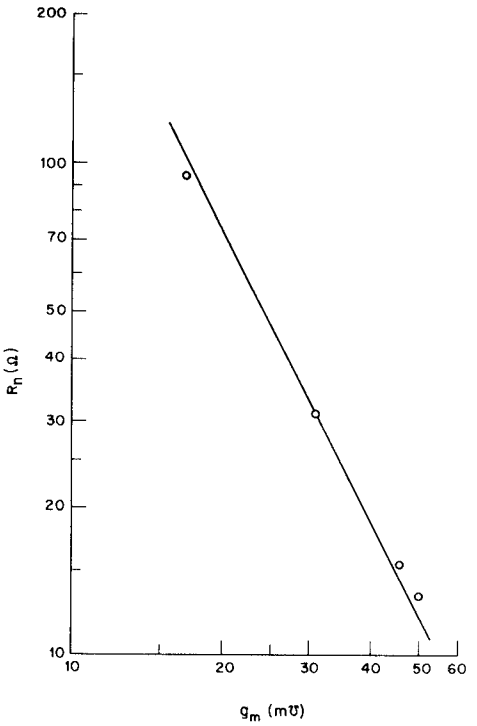

Fig. 3. Correlation between the equivalent noise resistance R_n and transconductance g_m.

$$R_{op} = k_3\left[\frac{1}{4g_m} + R_g + R_s\right] \tag{4}$$

$$X_{op} = \frac{k_4}{fC_{gs}} \tag{5}$$

where k_1, k_2, k_3, and k_4 are fitting factors, and f is frequency.

Comparing these expressions with the experimental data shown in Table II would yield determination of the fitting factors. As seen in Figs. 2–5, it has been found that the expressions would well represent the measured values of the noise parameters if the fitting factors were chosen as follows:

$$k_1 = 0.016$$
$$k_2 = 0.030$$

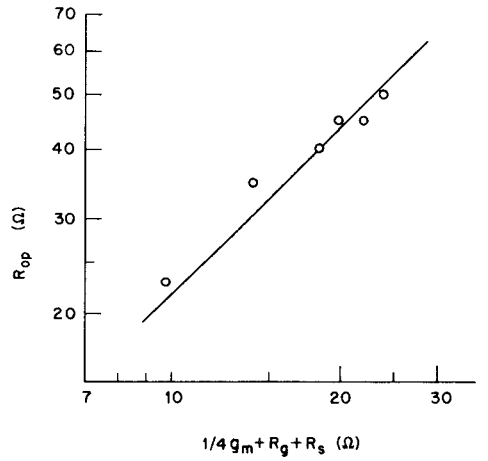

Fig. 4. Correlation between the optimum source resistance R_{op} and equivalent circuit elements g_m, R_g, and R_s.

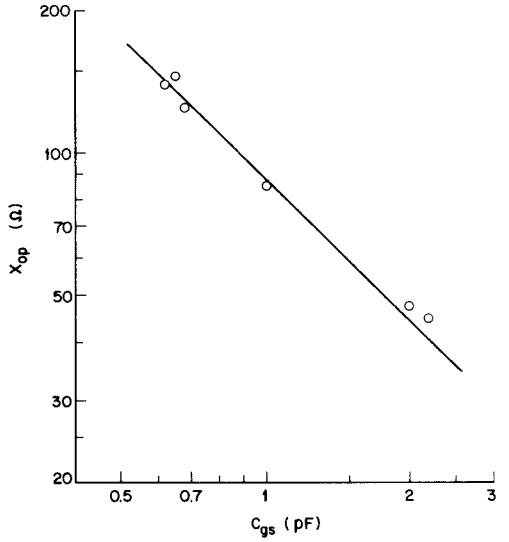

Fig. 5. Correlation between the optimum source reactance X_{op} and gate-source capacitance C_{gs}.

$$k_3 = 2.2$$

$$k_4 = 160$$

provided that R_n, R_{op}, X_{op}, R_g, and R_s are all in ohms, g_m in mhos, C_{gs} in picofarads, and f in gigahertz.

It may be remarked that the equivalent circuit elements as obtained with null gate bias are used in the above expressions for the noise parameters, although the noise parameters are provided with a certain gate bias. In spite of such a difference in the gate-bias conditions, the above relationships were empirically found to be present. If the equivalent circuit elements were measured under a gate-bias condition different from the null gate bias, the fitting factors would have to be modified.

A deviation of X_{op}, with increasing C_{gs}, from the linear relationship as seen in Fig. 5 was probably caused by an increased participation of the input lead inductance in X_{op}.

C. Semiempirical Expressions for Transconductance, Gate-Source Capacitance, and Cutoff Frequency

For design purposes, g_m and C_{gs} must be expressed in terms of the geometrical and material parameters of a device. Approximate expressions were then derived on a semiempirical basis as follows:

$$g_m = k_5 Z \left[\frac{N}{aL} \right]^{1/3} \mho \tag{6}$$

$$C_{gs} = k_6 Z \left[\frac{NL^2}{a} \right]^{1/3} \text{pF} \tag{7}$$

$$f_T = \frac{10^3 g_m}{2\pi C_{gs}} = \frac{9.4}{L} \text{ GHz} \tag{8}$$

in which fitting factors k_5 and k_6 were found to be 0.020 and 0.34, respectively, for the sample devices under the zero gate-bias condition.

Figs. 6 and 7 show comparisons of g_m and C_{gs}, respectively, between the calculated values using L, N, and a given in Table I and the measured values shown in Table II. They are in good agreement in both cases.

D. Simplified Expressions for Parasitic Resistances

Simplified expressions for R_g and R_s of the sample MESFET's would be given by [11]

$$R_g = \frac{17z^2}{hLZ} \ \Omega \tag{9}$$

$$R_s = \frac{1}{Z}\left[\frac{2.1}{a^{0.5}N^{0.66}} + \frac{1.1L_{sg}}{(a-a_s)N^{0.82}} \right] \Omega \tag{10}$$

where h is the gate metallization height in micrometers, L_{sg} is the distance between the source and gate electrodes in micrometers, and a_s is the depletion layer thickness in micrometers at the surface in the source-gate space.

E. Practical Expressions for Noise Parameters

The substitution of (6)–(10) into (2)–(5) in association with the practical values of the fitting factors yields

$$F_{\min} = 1 + 0.038f\left[\frac{NL^5}{a} \right]^{1/6} \cdot \left[\frac{17z^2}{hL} + \frac{2.1}{a^{0.5}N^{0.66}} + \frac{1.1L_{sg}}{(a-a_s)N^{0.82}} \right]^{1/2} \tag{11}$$

$$R_n = 75Z^{-2}\left[\frac{aL}{N} \right]^{2/3} \Omega \tag{12}$$

$$R_{op} = 2.2Z^{-1}\left[12.5\left(\frac{aL}{N} \right)^{1/3} + \frac{17z^2}{hL} + \frac{2.1}{a^{0.5}N^{0.66}} + \frac{1.1L_{sg}}{(a-a_s)N^{0.82}} \right] \Omega \tag{13}$$

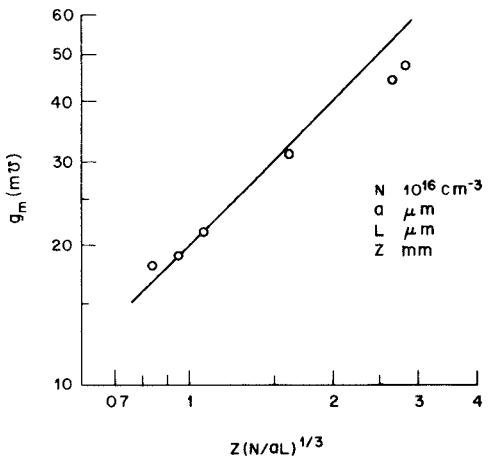

Fig. 6. Transconductance g_m as a function of channel parameters Z, L, a, and N.

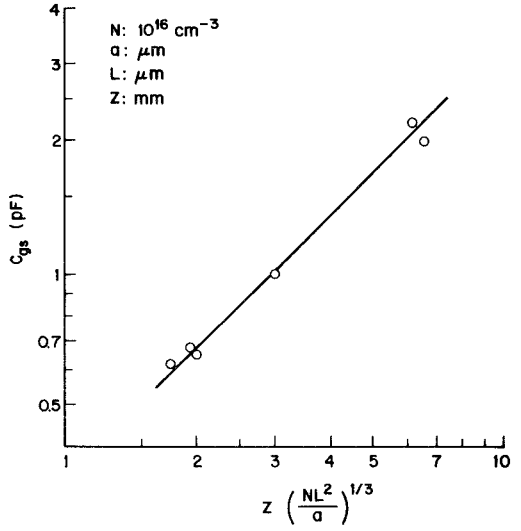

Fig. 7. Gate-source capacitance C_{gs} as a function of channel parameters Z, L, a, and N.

$$X_{op}=\frac{450}{fZ}\left[\frac{a}{NL^2}\right]^{1/3}\Omega. \tag{14}$$

Again, units are gigahertz (GHz) for f, millimeter (mm) for z and Z, micrometer (μm) for a, a_s, h, L, and L_{sg}, and 10^{16} cm^{-3} for N.

Since $F_{\min}$ is dominated by the parasitic resistances outside the gate region, $F_{\min}$ is structure sensitive [12]. Remember that (11) is suitable for the simplest structure of MESFET's. As sophistication increases in the structure, the proper expression for $F_{\min}$ may be obtained after the corresponding modification primarily to (10), and hence to (11). Applications of the gate recess structure [8], [12] and n^+-GaAs epitaxial layer [13] are the major examples of structural variations so far reported.

In (12), it is seen that *a small R_n value can be obtained with a short gate device having a heavily doped thin active channel.* The expression for R_n given in (12) may hold, regardless of the structural modification applied to a section of the channel outside the gate region.

IV. Discussions on Minimum Noise Figure, Associated Power Gain, and Input Impedance Match

A. Example 1

In order to see the characteristic variations of $F_{\min}$ and R_n as functions of N and a, the following conditions are assumed:

$$L=L_{sg}=1.0\ \mu\text{m}$$
$$R_g=4.0\ \Omega$$
$$f=0.4f_T=3.76\ \text{GHz}.$$

Furthermore, a_s is assumed to be approximately equal to the gate depletion layer thickness under null gate-bias condition a_0 in numerical value. This parameter has been given by [11]

$$a_0=\left[\frac{0.706+0.06\log N}{7.23N}\right]^{1/2}\mu\text{m}$$

for aluminum gates, as far as $a>a_0$. Under such conditions, (11) reduces to

$$F_{\min}|_{f=0.4f_T}=1+0.15[N/a]^{1/6}\cdot\left[1.82+\frac{1.9}{a^{0.5}N^{0.66}}+\frac{1}{(a-a_0)N^{0.82}}\right]^{1/2}. \tag{15}$$

The calculated values of $F_{\min}$ by (15) and of R_n by (12) are shown in Fig. 8, both as the contour mapping on the a-N plane. It can be seen that $F_{\min}$ is a weak function of N for a given value of a. Also, $F_{\min}$ takes a low value in the region where the a/N ratio is high. This is the contradictory condition to obtaining the low value of R_n. The high a/N ratio tends to provide not only the critical noise tuning but also the low power gain. Therefore, there is a compromise in choosing a and N for the best overall performance as an amplifying device.

In Fig. 8, there are two other curves, as shown with the dash–dotted line, which indicate practical limits for the selection of a and N. The upper curve corresponds to the a and N values which provide a drain–source breakdown voltage V_B, of 10 V if the gate is biased at the pinchoff voltage, $-V_p$. The lower curve indicates the thickness of the gate depletion layer at zero bias for aluminum gates.

B. Example 2

In order to see a clear distinction between the low a/N device and high a/N device, the following two representatives were assumed under the same conditions, as used in the previous section.

Device A: $N=12.5\times10^{16}$ cm^{-3} and $a=0.2\ \mu$m.
Device B: $N=5.0\times10^{16}$ cm^{-3} and $a=0.5\ \mu$m.

The noise performance of these devices was calculated using (12)–(15). The results are then plotted on the signal

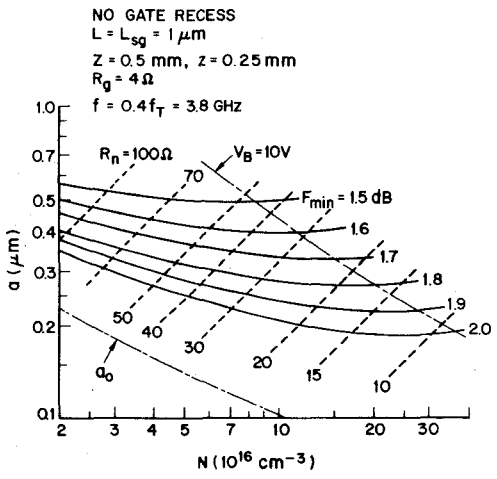

Fig. 8. Contours of equi-F_{min} and equi-R_n on the a-N plane for 1-μm gate devices.

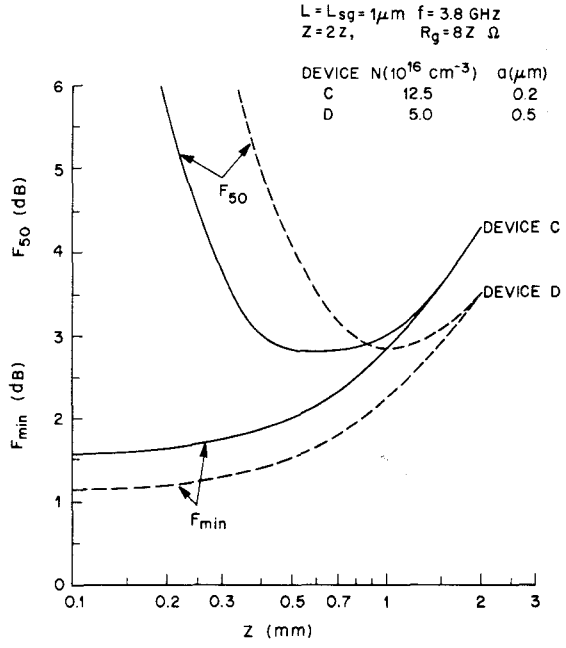

Fig. 10. Noise figures F_{min} and F_{50} as functions of total device width Z for two 1-μm gate devices.

$L = L_{sg} = 1\mu m$	DEVICE	$N(10^{16}cm^{-3})$	$a(\mu m)$
$Z = 0.5mm$, $z = 0.25mm$	----- A	12.5	0.2
$R_g = 4\Omega$, $f = 3.8$ GHz	—— B	5.0	0.5
$Z_0 = 50\Omega$			

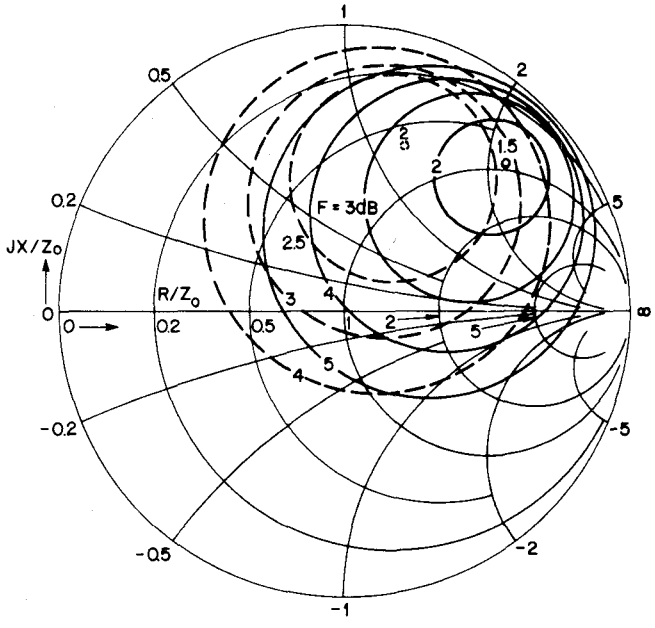

Fig. 9. The noise performance chart for two 1-μm gate devices.

source impedance chart [3], as shown in Fig. 9. It may be concluded that device B may reach the better noise performance in the case of a narrow-band application with the individually designed circuitry. However, device A may be more suitable in such a case that relatively large tolerances for the impedance variation are demanded. In addition, device A usually gives gain higher than that of device B, because of the higher value of g_m with device A.

C. Example 3

As seen in Fig. 9, device B, in spite of the smaller value of F_{min}, would exhibit much worse noise figure than device A when they are simply inserted into a 50-Ω coaxial system. Such a 50-Ω system insertion noise figure can be designated as F_{50}, which is

$$F_{50} = F_{min} + \frac{R_n}{50}\left[\frac{(50-R_{op})^2 + X_{op}^2}{R_{op}^2 + X_{op}^2}\right]. \tag{16}$$

Next shown are the dependence of F_{min} and F_{50} on Z, provided that $Z = 2z$. Two representative devices C and D were chosen, which were the same as devices A and B, respectively, except for an additional assumption that $R_g = 8Z$, in which R_g is in units of ohms and Z is in millimeters. Parameters F_{min} and F_{50} were then calculated as functions of Z, using (11)–(14) and (16). The results are shown in Fig. 10, in which F_{min} gradually increases with increasing Z for both devices. On the contrary, F_{50} varies as a strong function of Z and takes a minimum for moderate values of Z, as also shown in Fig. 10. For the overall performance as a general purpose low-noise MESFET with two paralleled unit-gates 1 μm long, an optimum value of the total gate width could be evaluated to be 0.4–0.5 mm for device C, and 0.8–1.0 mm for device D.

D. Example 4

In [14], the noise and gain performance as measured at 8 GHz for GaAs MESFET's with 0.5-μm-long gates was described. The device consists of four sections of 70-μm-wide units, i.e., $z = 0.07$ mm and $Z = 0.28$ mm. The height of aluminum as the gate metallization was 0.5 μm. The source-to-gate distance was 0.8 μm. The active layer thickness was claimed to be between 0.1 and 0.2 μm. The gate pinchoff voltage V_p of typical devices was 2.0 V. Since the representative value of N was 25×10^{16} cm^{-3}, the corre-

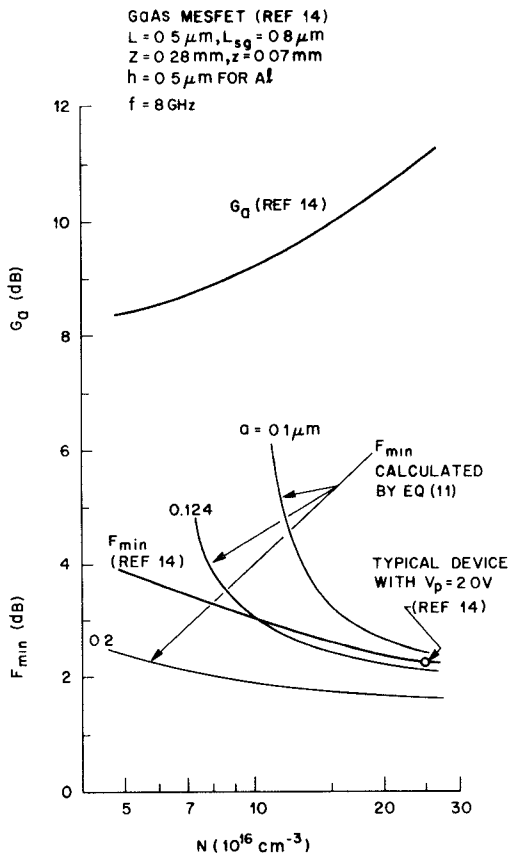

Fig. 11. Calculated values of F_{min} and measured values of F_{min} and associated power gain G_a for 0.5-μm gate devices.

sponding value of a was evaluated to be 0.124 μm. Thus F_{min} at 8 GHz was calculated using (11) as a function of N for the three values of a, i.e., 0.1, 0.124, and 0.2 μm.

As shown in Fig. 11, the measured F_{min} values happened to be between the two calculated curves of F_{min} for $a=0.1$ and 0.2 μm. Moreover, the measured F_{min} for $N \geqslant 10\times10^{16}$ cm^{-3} agreed well with the calculated F_{min} for $a=0.124$ μm. However, the measured F_{min} for $N<10\times10^{16}$ cm^{-3} appeared to be better than the calculated F_{min} for $a=0.124$ μm. This discrepancy could have been caused by an increased active layer thickness of the actual devices with $N<10\times10^{16}$ cm^{-3}, in order to maintain the zero gate-bias drain current to be finite in the positive direction. Such an increase in a should result in an improvement of F_{min} from that predicted for $a=0.124$ μm, as seen in Fig. 11. Therefore, it can be concluded that the experimental data on the noise performance, [14, fig. 2], is well explained by (11) of this paper.

In the same reference figure as mentioned above the associated power gain G_a, was also shown as a function of N. The data are replotted in Fig. 11 in which G_a increases with increasing N and hence N/a, as has been predicted in the previous sections of this paper.

E. Remarks

In general, with increasing N/a, G_a increases and R_n decreases. If R_g is small enough as compared to R_s, F_{min} is improved with an increased value of N for a given value of a. This has been empirically known in the industry [15]. The reason is that R_s dominates F_{min} for a given value of L, and that R_s decreases with increasing the Na product. In the simple planar channel structure used here, F_{min} increases with decreasing a for a given N. However, in a sophisticated channel structure, this may no longer hold partly due to a possible decrease in the effective gate length [11], [13].

V. Conclusions

A set of four noise parameters for GaAs MESFET's of the planar channel structure were semiempirically found in terms of simple functions of its equivalent circuit elements. Each of the equivalent circuit elements was further expressed by the device geometrical and material parameters in a simple analytical form. Combining these two things together yielded the practical expressions for the four noise parameters in terms of the device geometrical and material parameters.

Among the four noise parameters, F_{min} and R_n were regarded as most crucial for a device to be used in a broad-band low-noise amplifier. Because a device with a small value of R_n behaves rather insensitively to the variation in the signal source impedance, the variation in the noise figure over the band can be expected to be small. In addition, as the inverse of R_n is closely related to power gain, smaller R_n can enhance the gain performance.

The aforementioned expression for R_n indicates that a small value of R_n can be obtained with a short gate device having a heavily doped thin active channel (i.e., a high N/a ratio). This is, in general, the contradictory condition to obtaining a low value of F_{min}. Although F_{min} is a weak function of N for a given value of a, F_{min} takes a low value in the region where the N/a ratio is low. However, the low N/a ratio tends to make the noise tuning critical and to degrade the power gain. Therefore, a compromise in choosing a and N is necessary for the best overall amplifier performance.

The proper selection of a and N may vary depending upon the particular purpose of an amplifier. Four examples were given to show the dependence of the noise, gain and input matching properties on a and N in a practical manner. If the gate metallization resistance were designed to be small enough to the total source series resistance, the minimum noise figure, associated power gain, and input matching sensitivity would all be improved with increasing N for a given a. This is a case which has been often observed in the industry.

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Continuous Varactor-Diode Phase Shifter with Optimized Frequency Response

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***Abstract*—A method is introduced for designing continuous varactor-diode phase shifters with optimum frequency response. The circuit used gives very small frequency variations of the phase shift if the maximum phase shift of the device is less than about 200°. Measurement results on a 180° *L*-band phase shifter are presented. This unit gives less than 5° variation of any given phase shift less than 180°, when the frequency is changed from 1.5 to 1.7 GHz.**

I. INTRODUCTION

A PROBLEM in the design of continuous varactor-diode phase shifters which has not received previous attention is the optimum frequency behavior at all possible phase shifts. The frequency response is said to be optimum when the derivative of the phase shift with frequency is zero at the center frequency. In this paper the design of a 180° continuous phase shifter will be described, which is almost ideal in this respect.

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An interesting 360° varactor-diode phase shifter was introduced in 1971 by Henoch and Tamm [1]. The main parts of the design were two parallel coupled series resonant circuits which were connected to a circulator by means of a quarter-wave transformer. The purpose of the transformer was to equalize the insertion loss. The phase shifter was designed to give optimum frequency behavior at 360° phase shift, but computer simulation has shown large frequency dependence at phase shifts between 0° and 360°.

Starski [2] has reported on an increase in bandwidth for p-i-n-diode reflection-type phase shifters by choosing the length and the impedance of the transformer for optimum frequency response. An attempt was made to improve the continuous 360° shifter in this way, but it was not possible to decrease the frequency variations at all phase shifts to any large extent.

It was, therefore, decided to limit the maximum phase shift to less than 360° by changing one of the series resonant circuits. With an optimized transformer, this circuit has the required performance.

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